

MS-7678

CPU:

uATX

Ver: 1.1

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH

OnBoard Chipset:

Clock Gen:IDT 4105

HD Audio Codec:RTL892

LAN:RTL 8111E 10/100/1000

SIO:FIN71889ED

Flash ROM: 32 Mb SPI (PCH)

Main Memory:

DDR III (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 3

PWM:

Controller:VRD12 ISL6364CRZ 4+1-Phase

CPU+GPU

Controller:uP6138

CPU VTT CPU SA

Controller:uP6138

DDR PCH

ACPI:

UPI

SATA3.0X1 + e-SATA X1(MARVELL9128_COLAY_E9172)

USB2.0 RearX4 Front x8(PCH&BC Charge & i Charge)

USB3.0 RearX2 (NEC USB3.0)

1394 Controller - VT6315N-CE

D-SUB *1

DVI-D PORT*1

HDMI *1

TPM Header *1

COM Header *1

on BOARD BUZZER

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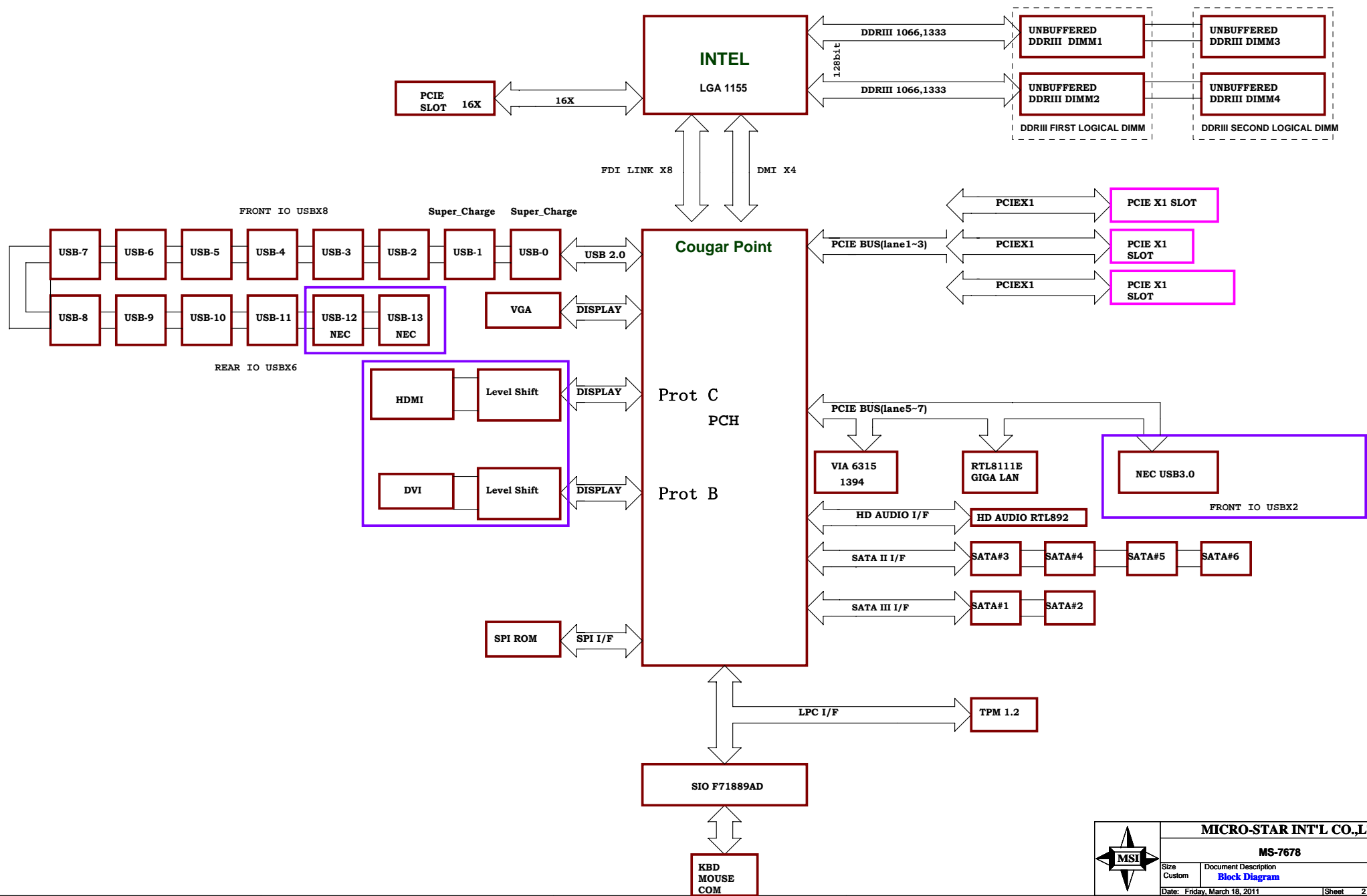
BOM OPT:

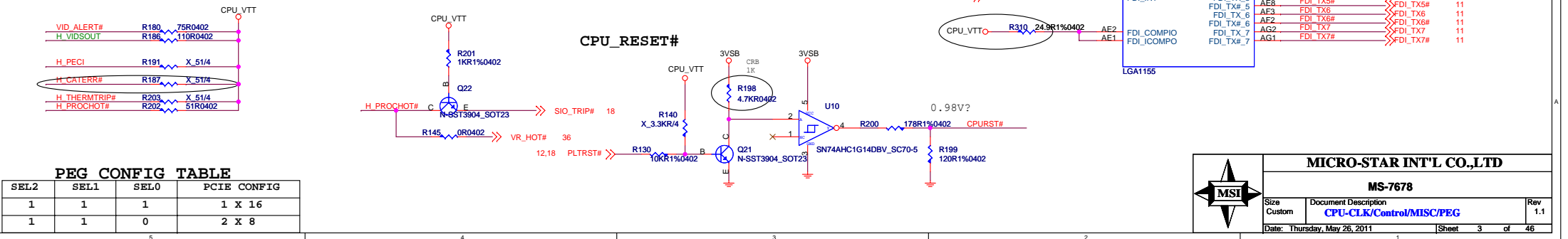
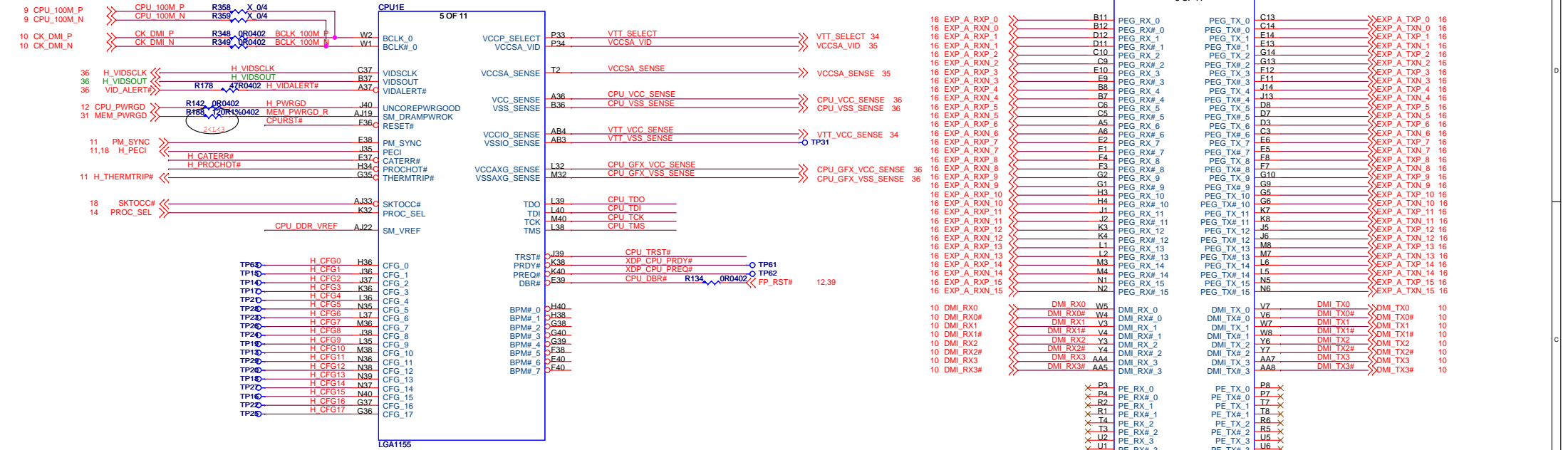
CFG-7678: STD H67MA-E45 01S

CFG-7678-A: A H67MA-S01 02S remove 1394\CD in\APS\HDMI\Rear SPDIF\Buzzer

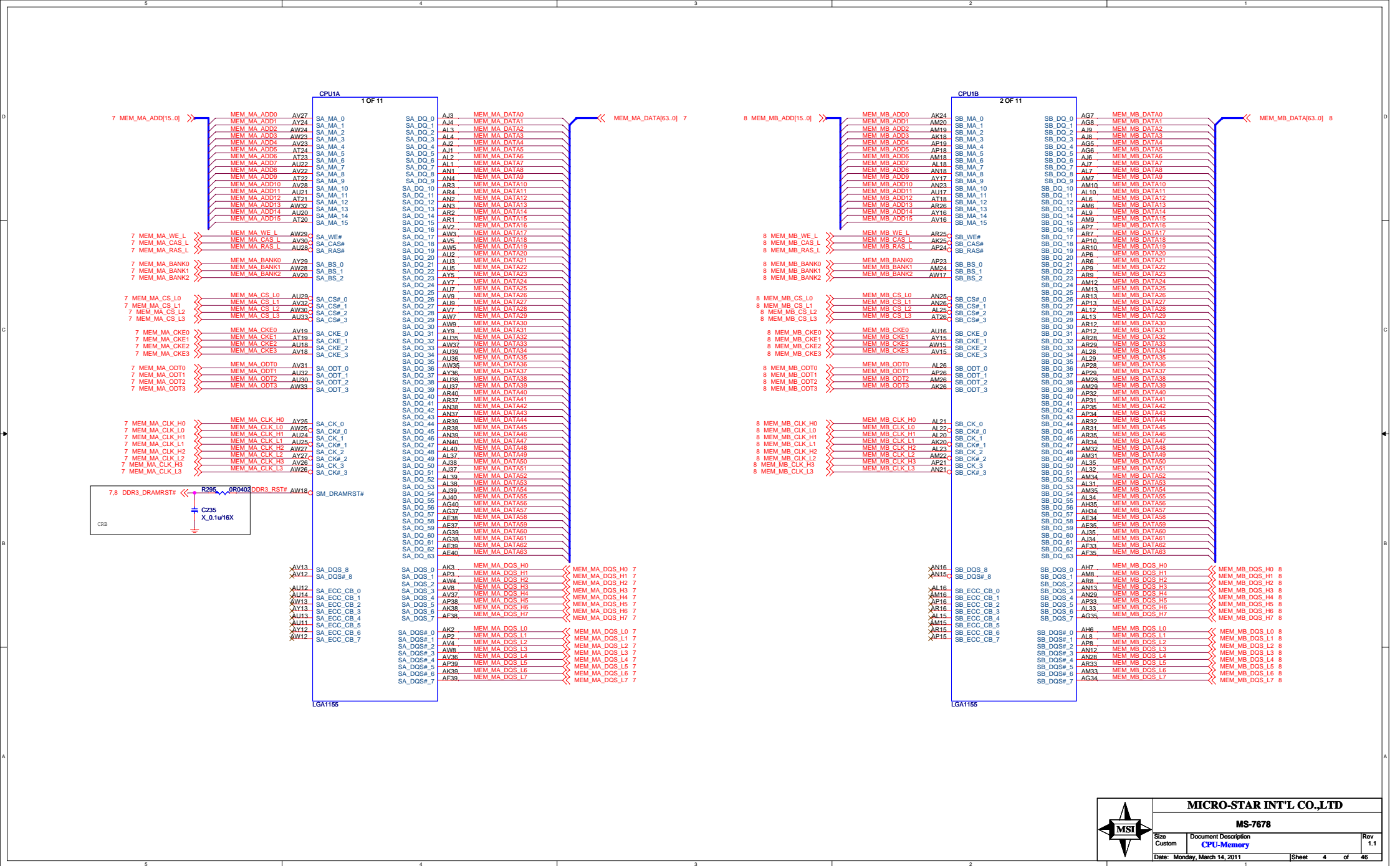
CFG-7678-B: B H67MS-E43 03S remove 1394\USB3.0

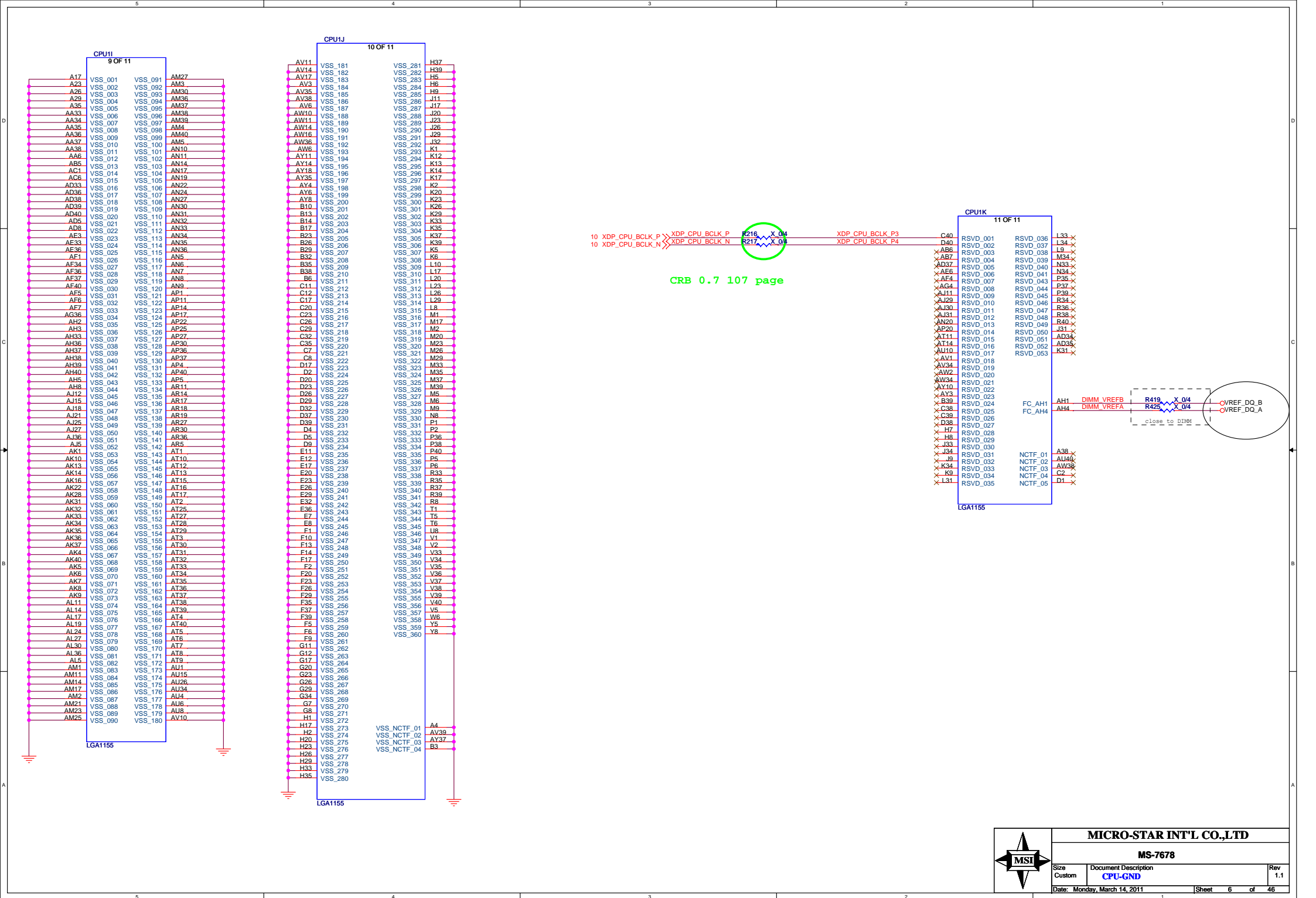
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| MICRO-STAR INT'L CO.,LTD | | |
| MS-7678 | | |
| Size Custom | Document Description Cover Sheet | Rev 1.1 |
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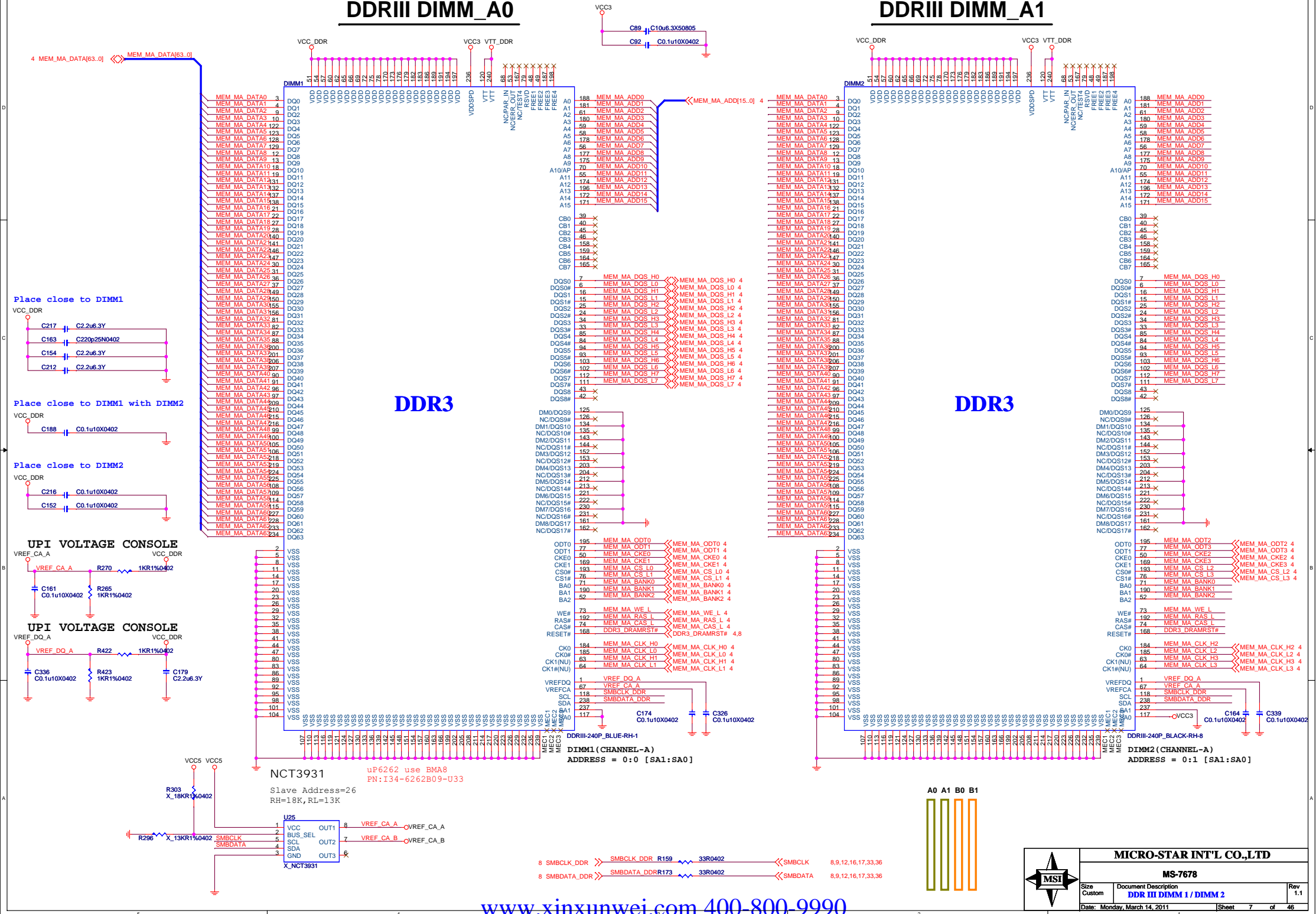
MICRO-STAR INT'L CO.,LTD
MS-7678
Size: Custom Document Description: CPU-CLK/Control/MISC/PEG Rev: 1.1
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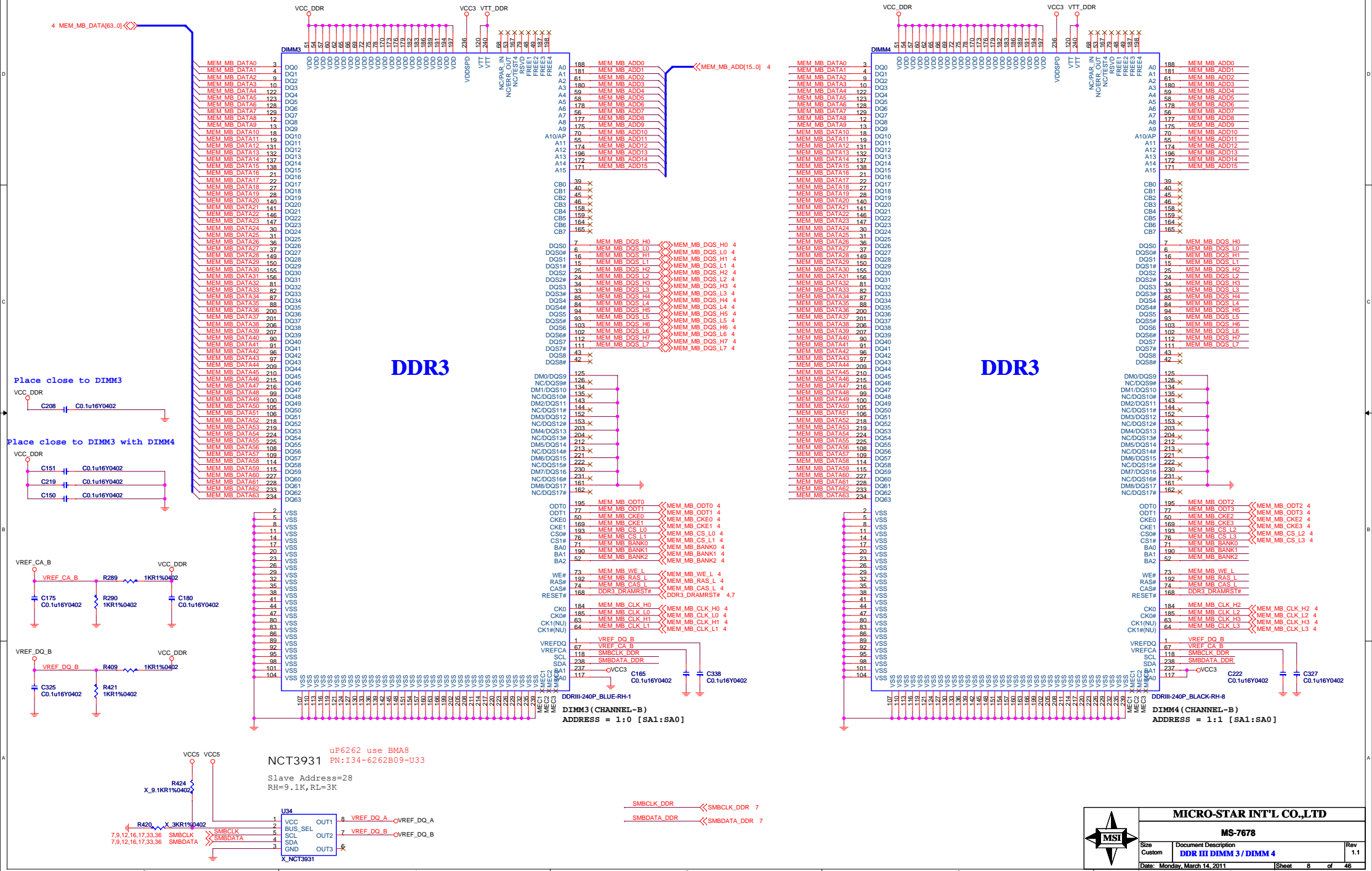
DDRIII DIMM_A0

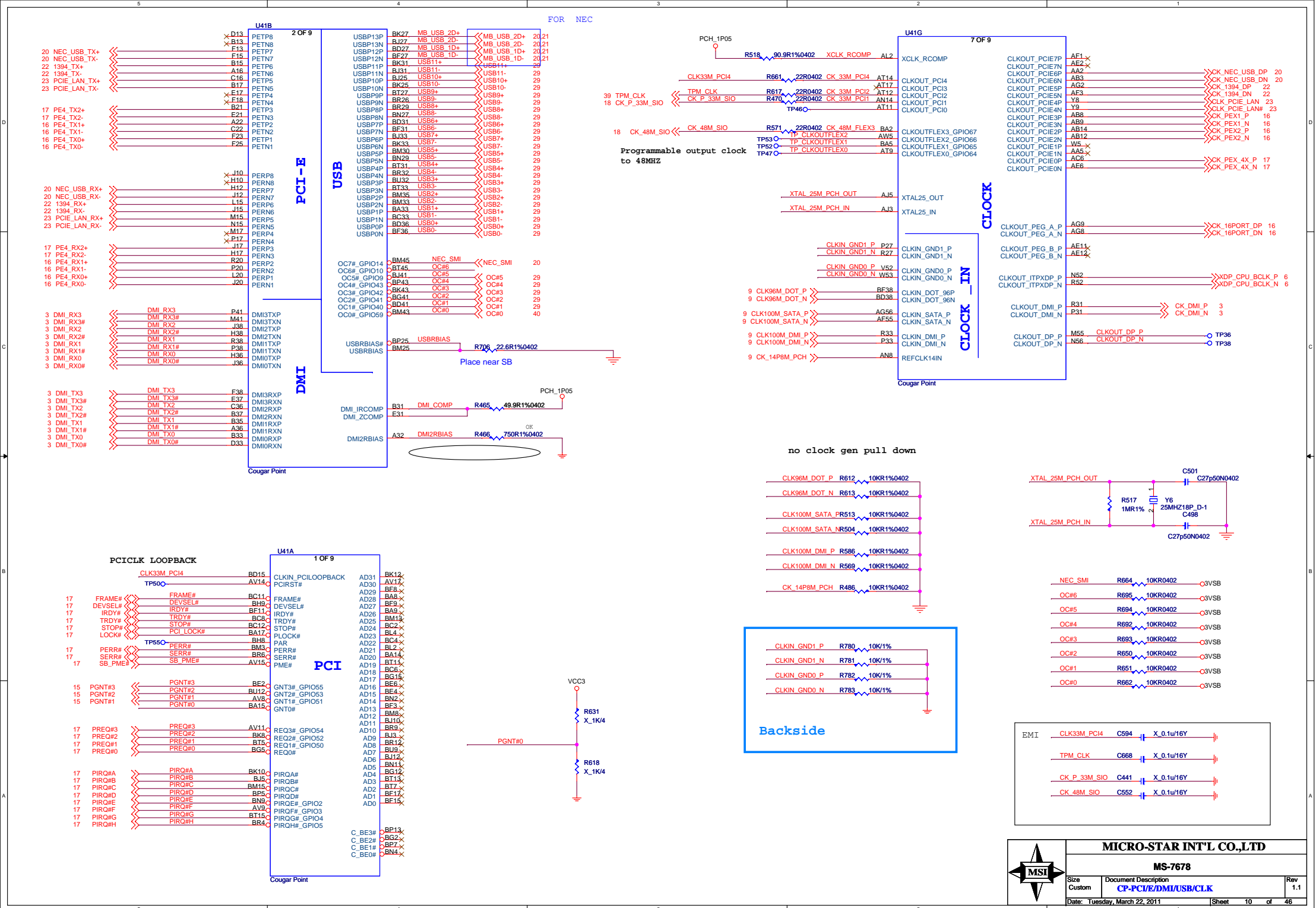
DDRIII DIMM_A1



DDRIII DIMM_B0

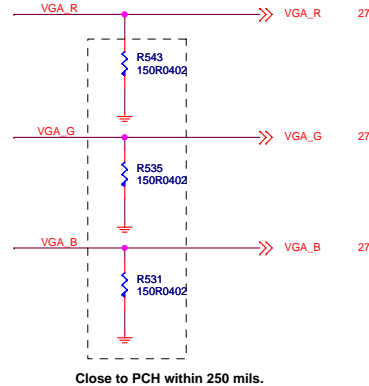
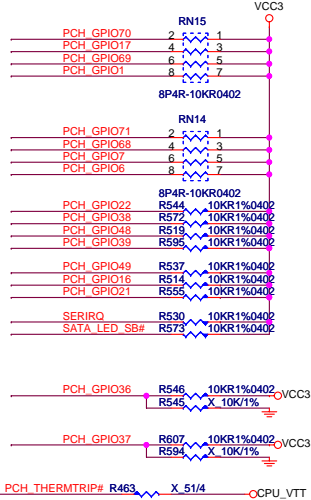
DDRIII DIMM_B1







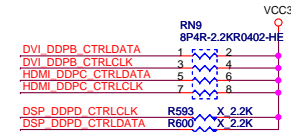
Pull HIGH for PCH



No VGA(pull down)



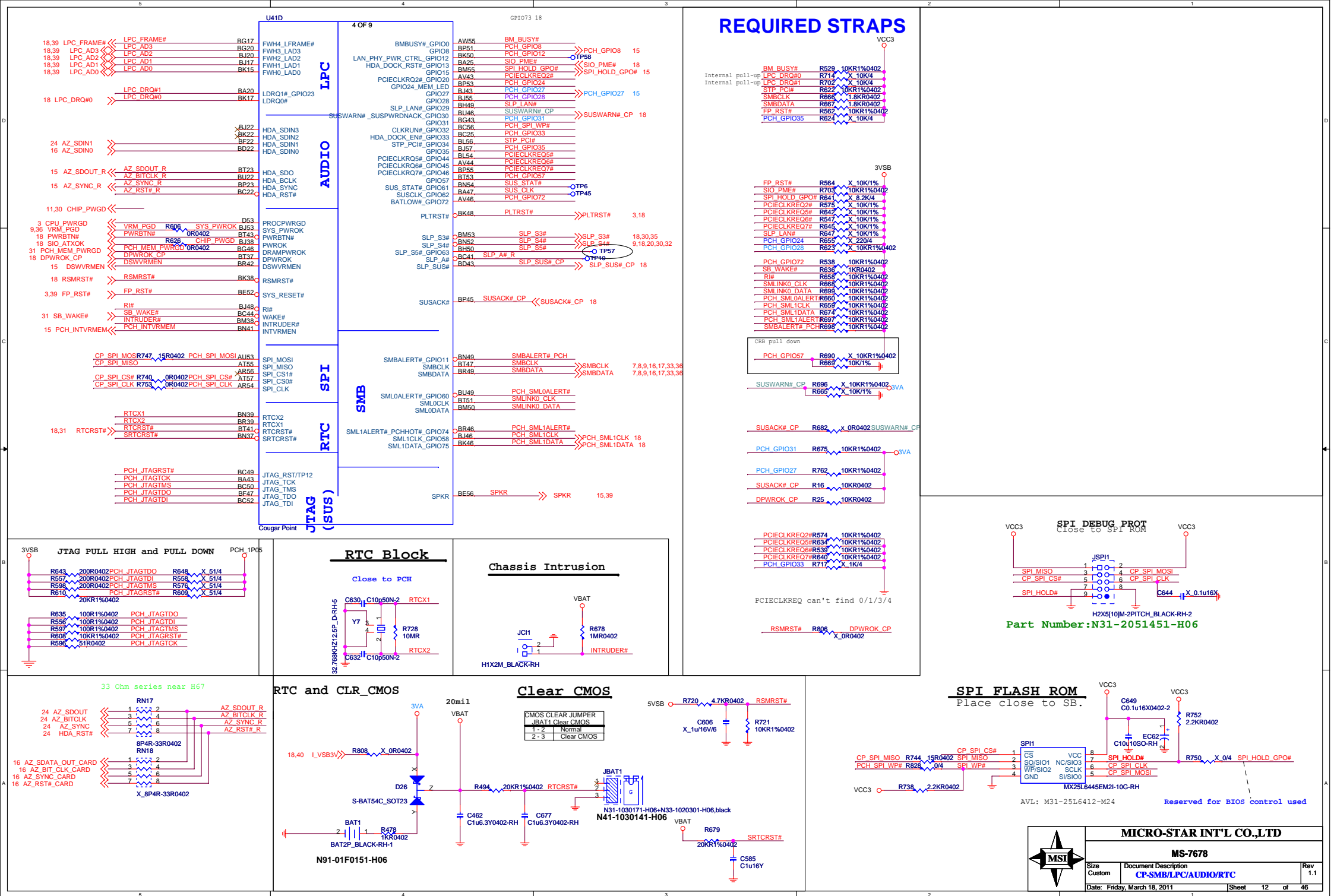
Enable VGA(CTRLCLK/DATA Pull High)

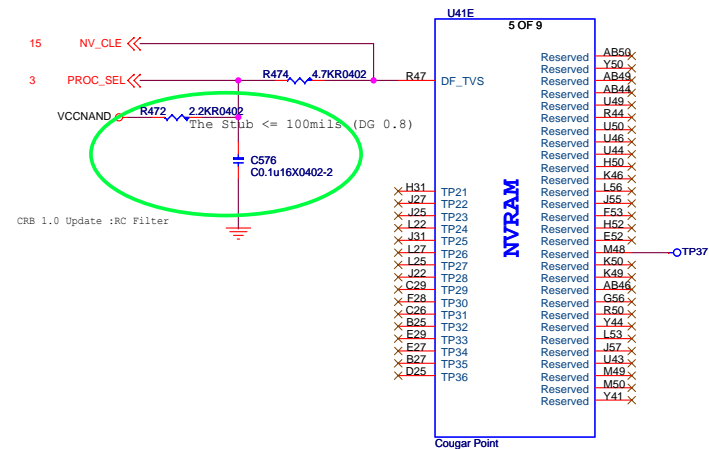
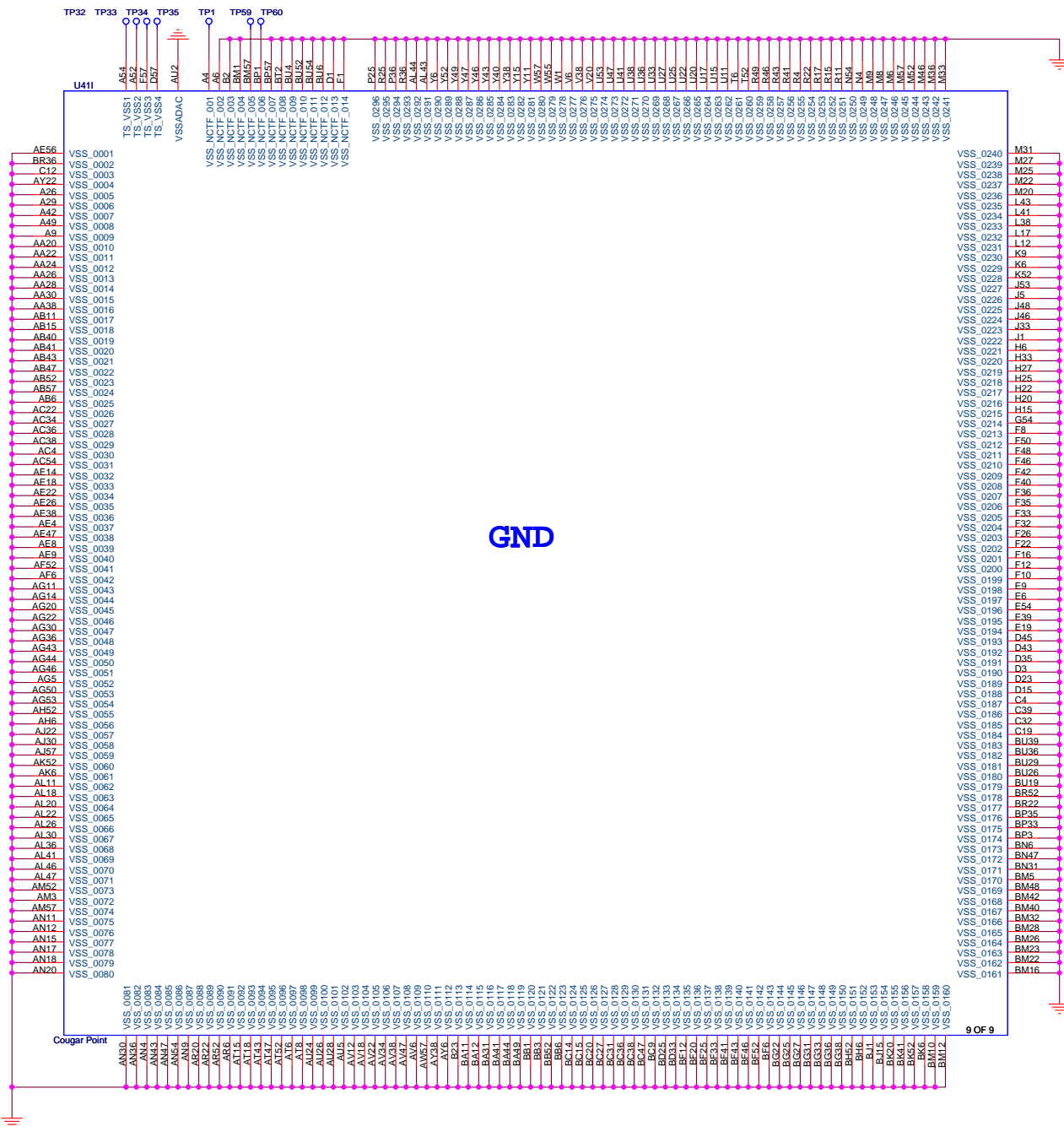


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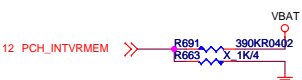
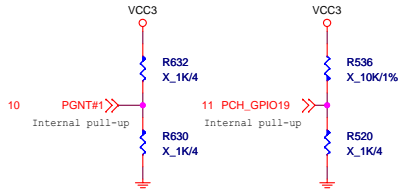
| Size | Document Description | Rev |
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| Custom | CP-SATA/HOST/FAN/GPIO/VGA | 1.1 |
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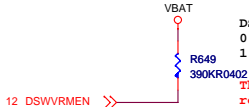
PCH Straps

| BOOT DEVICE | GNT1 | SATA1GP/GPIO19 |
|-------------|------|----------------|
| LPC | 0 | 0 |
| PCI | 1 | 0 |
| SPI | 1 | 1 |



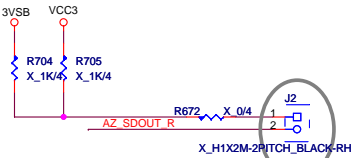
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



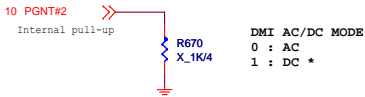
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

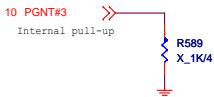


HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

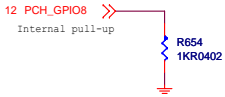
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



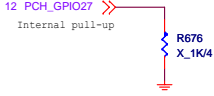
DMI AC/DC MODE
0 : AC
1 : DC *



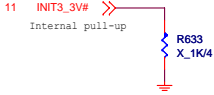
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

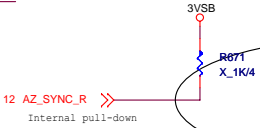


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ??????????????
1 : ?????????????? *

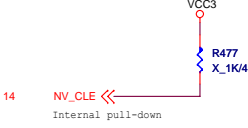
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



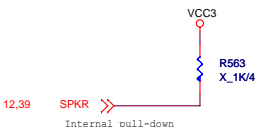
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



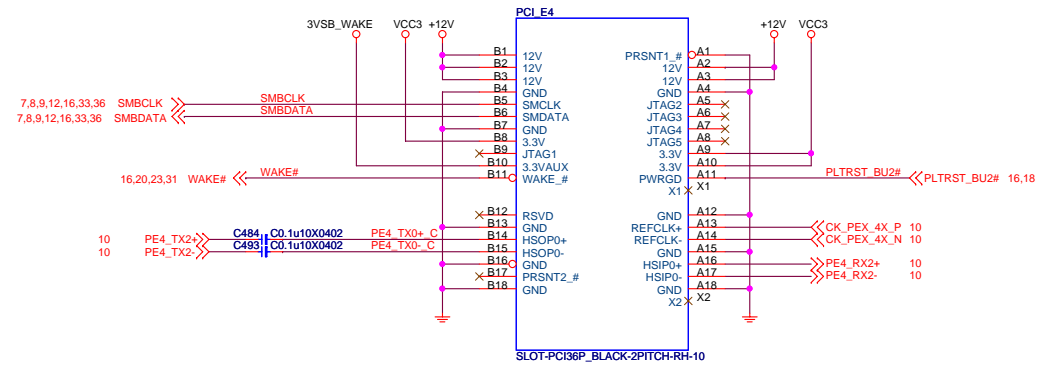
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

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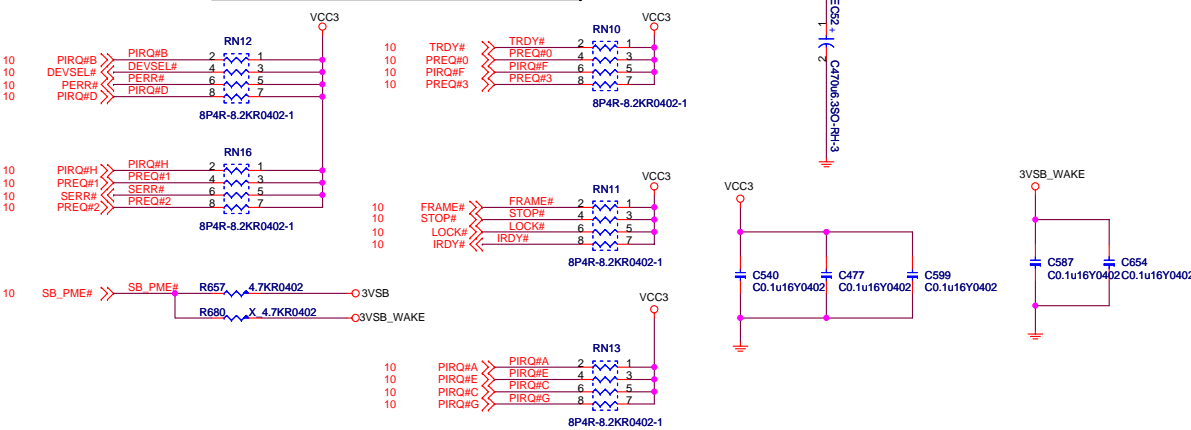
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| Custom | CP-Strap | 1.1 |
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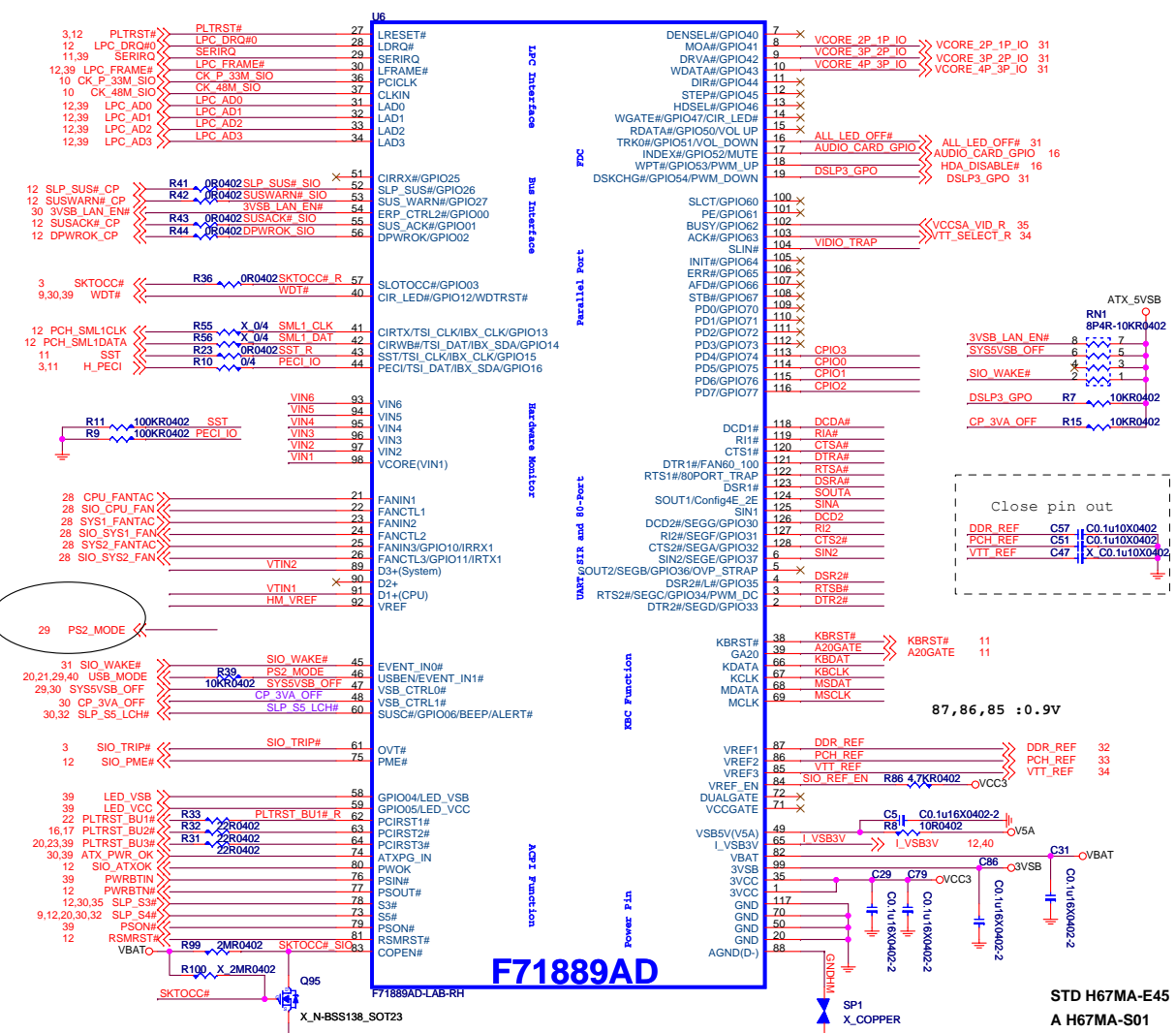
PCI EXPRESS x1-PORT



PCI PULL-UP / DOWN RESISTORS

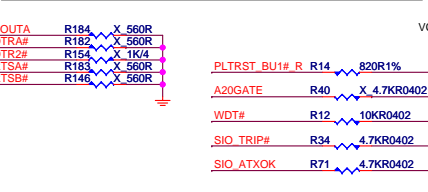


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| | MICRO-STAR INT'L CO.,LTD | | |
| | MS-7678 | | |
| | Size Custom | Document Description PCIEx1 Slots | Rev 1.1 |
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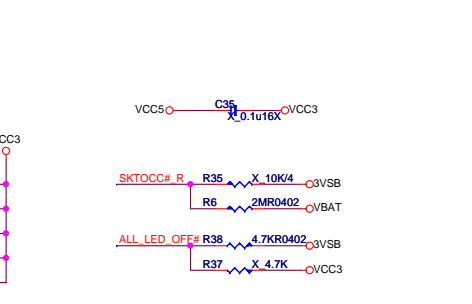


LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

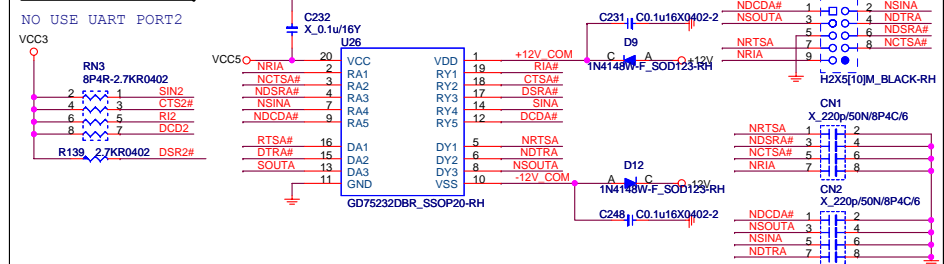
| STRAP | Don't STUFF | STUFF |
|-------|--------------------|---------------------|
| SOUTA | 4E | 2E |
| DTRA# | FAN START DUTY 60% | FAN START DUTY 100% |
| LDRQ# | PIN51~56=VID_OUT | PIN51~56=GPIO |
| DRRB# | SPI Backup | SPI Primary |
| RTSB# | PWM FAN | LINEAR FAN |
| RTSA# | 80 Port DISABLE | 80Port ENABLE |



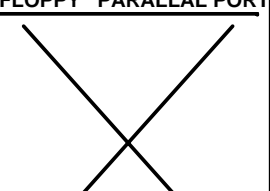
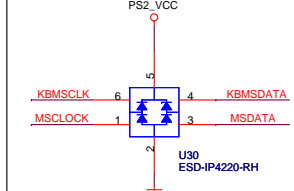
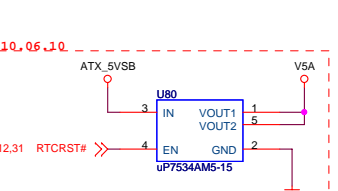
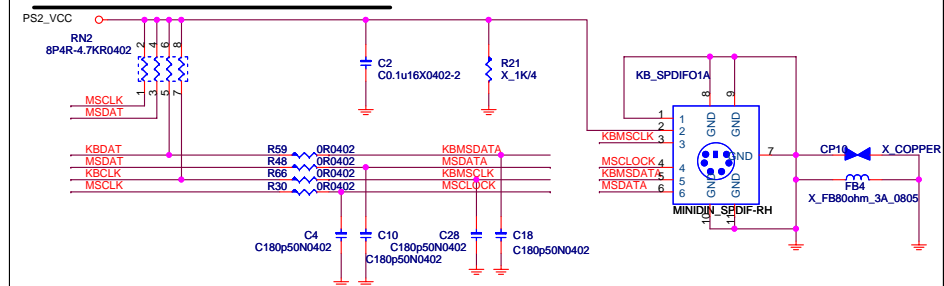
Pull down 47K:Pin 100-103 and pin 105-116 as GPIO pins



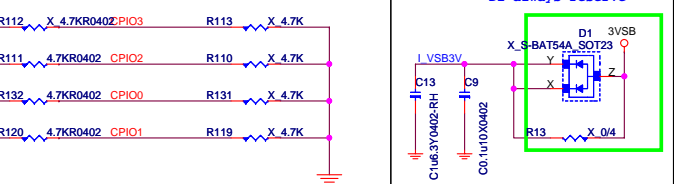
SERIAL PORT 1



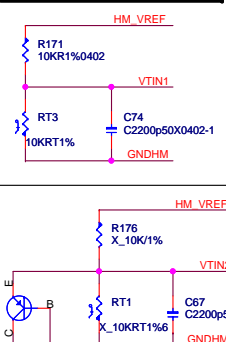
Dual in One PS2 Connector



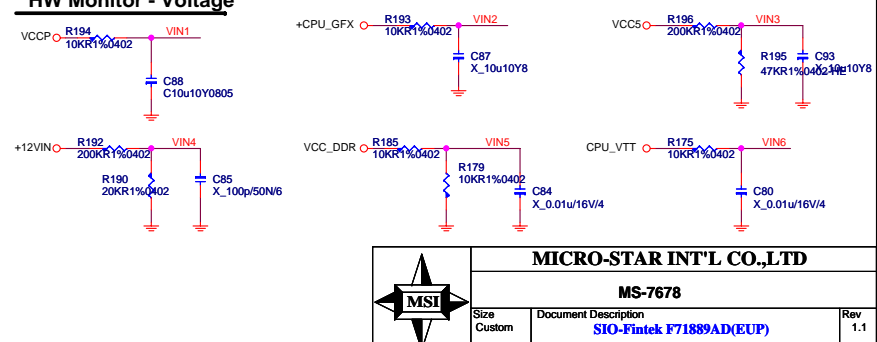
OPT BOM



HW Monitor - Thermal



HW Monitor - Voltage

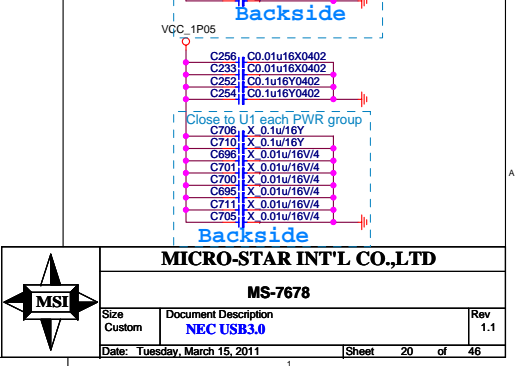
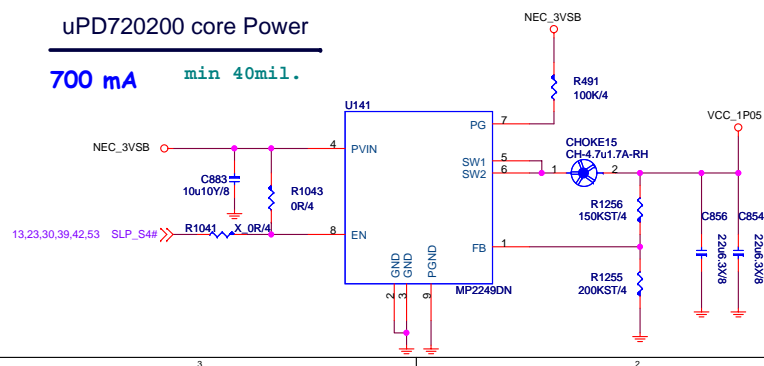
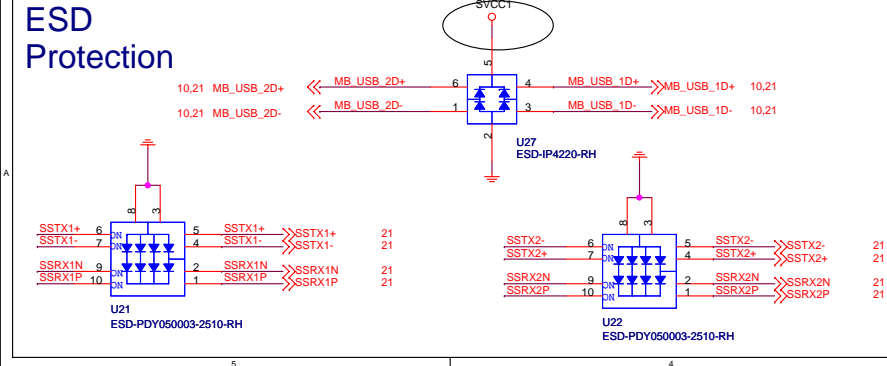
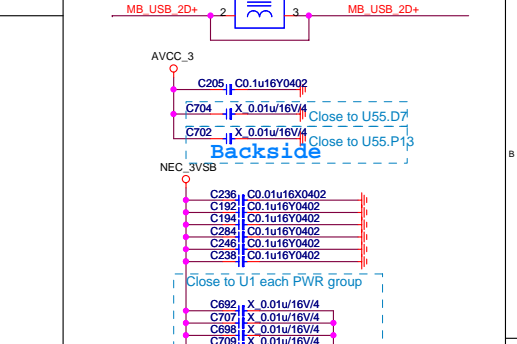
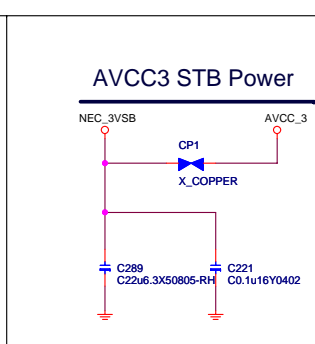
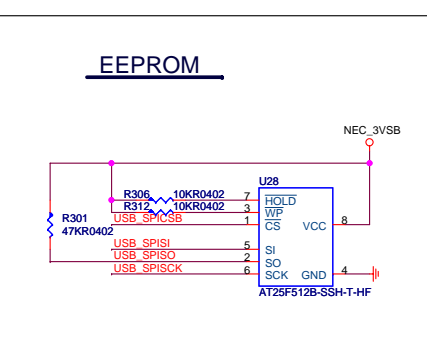
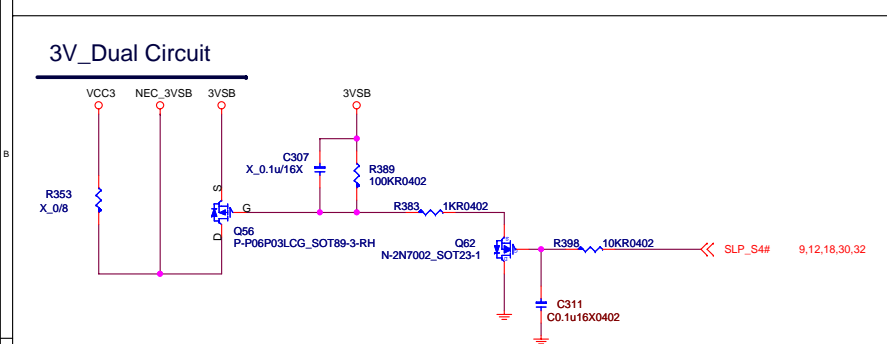
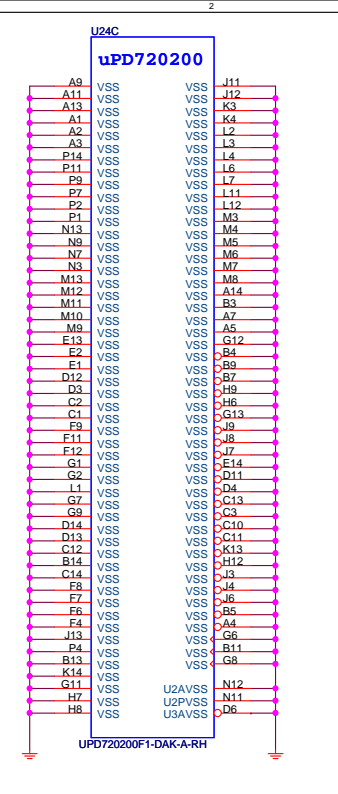
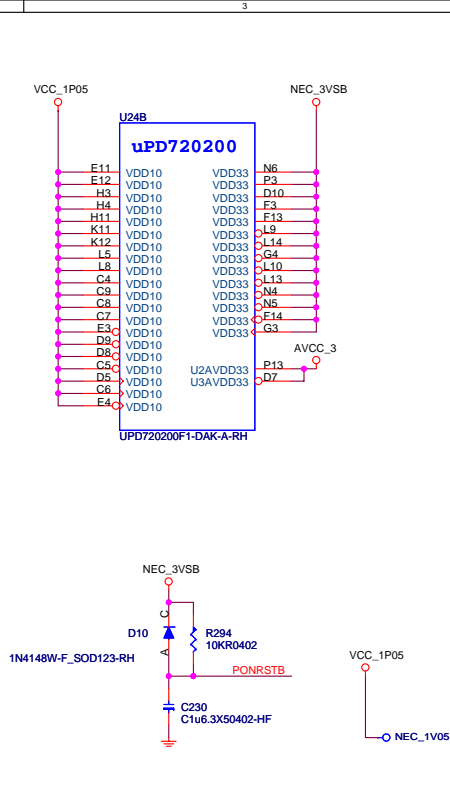


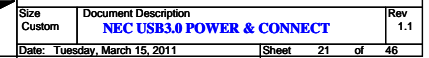
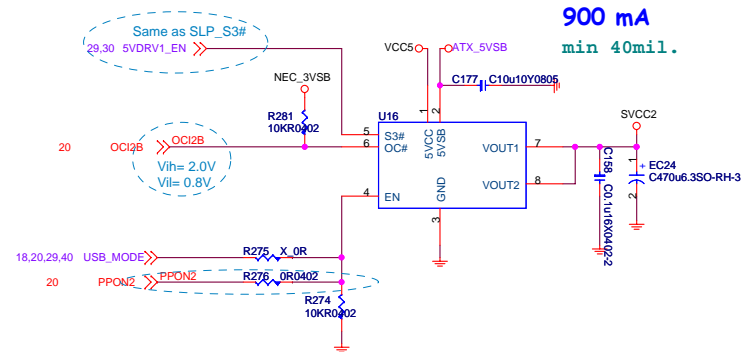
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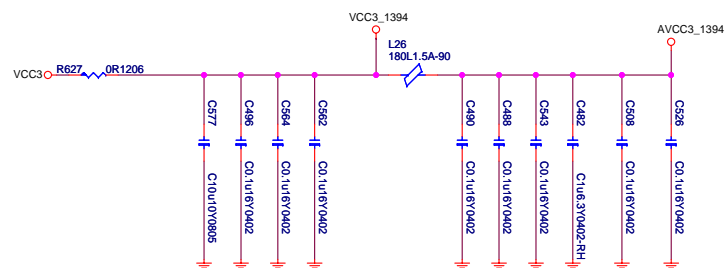
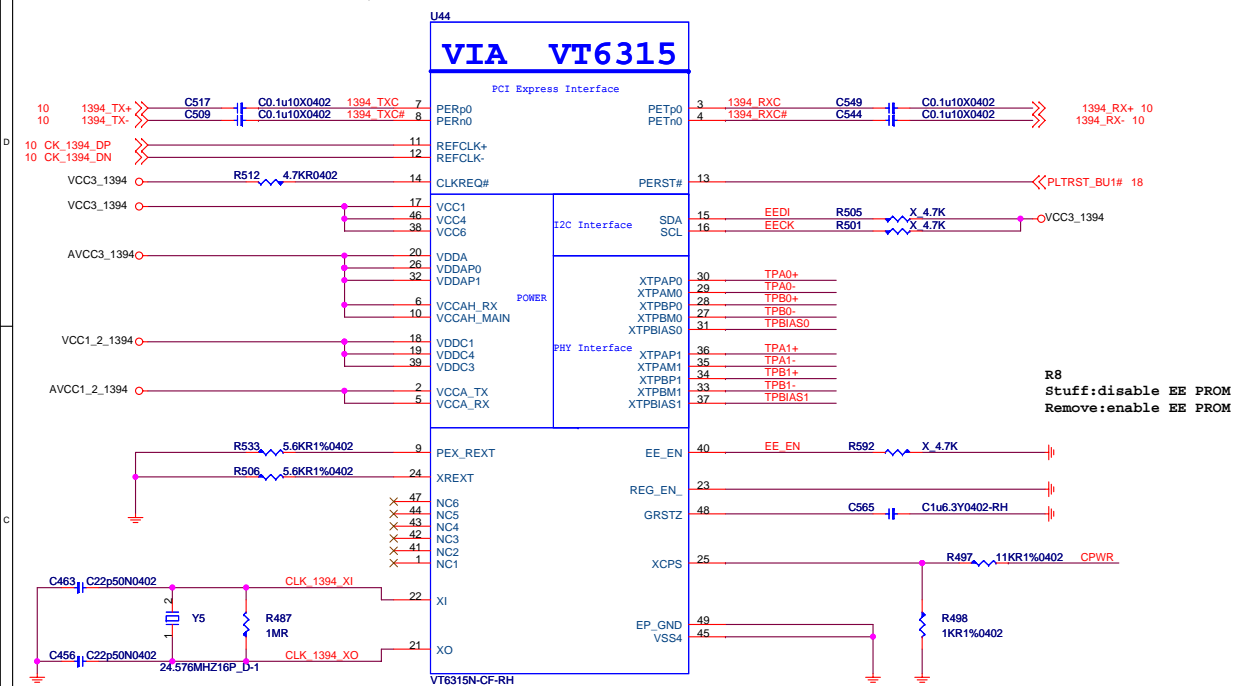
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| Size | Document Description | Rev |
| Custom | SIO-Fintek F71889AD(EUP) | 1.1 |

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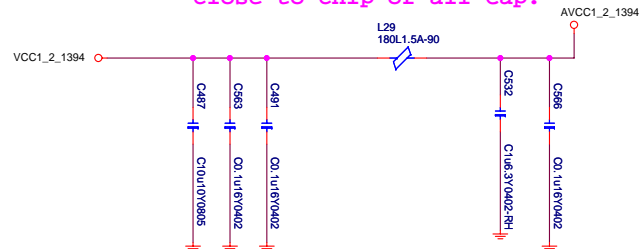




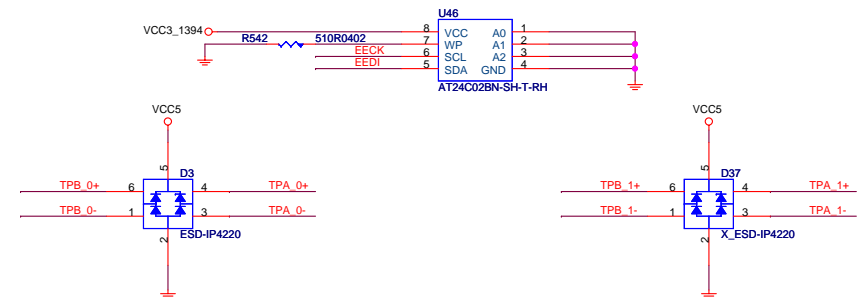
1394 CONTROLLER



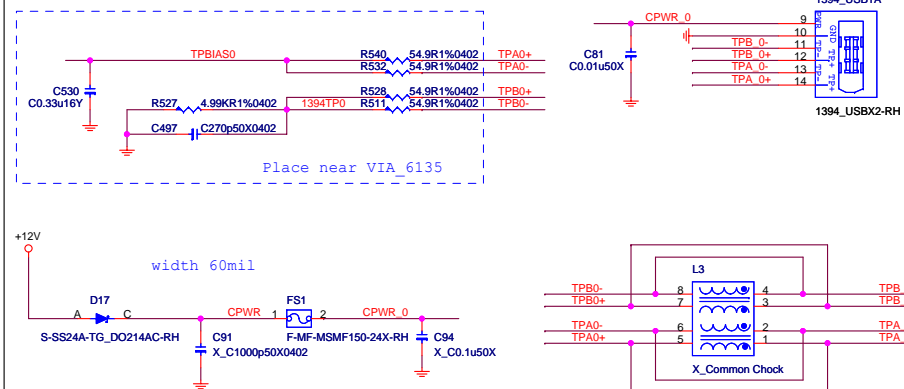
close to chip of all Cap.



EE PROM

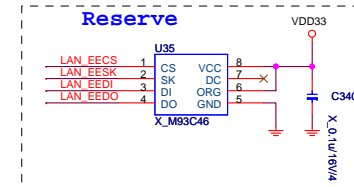
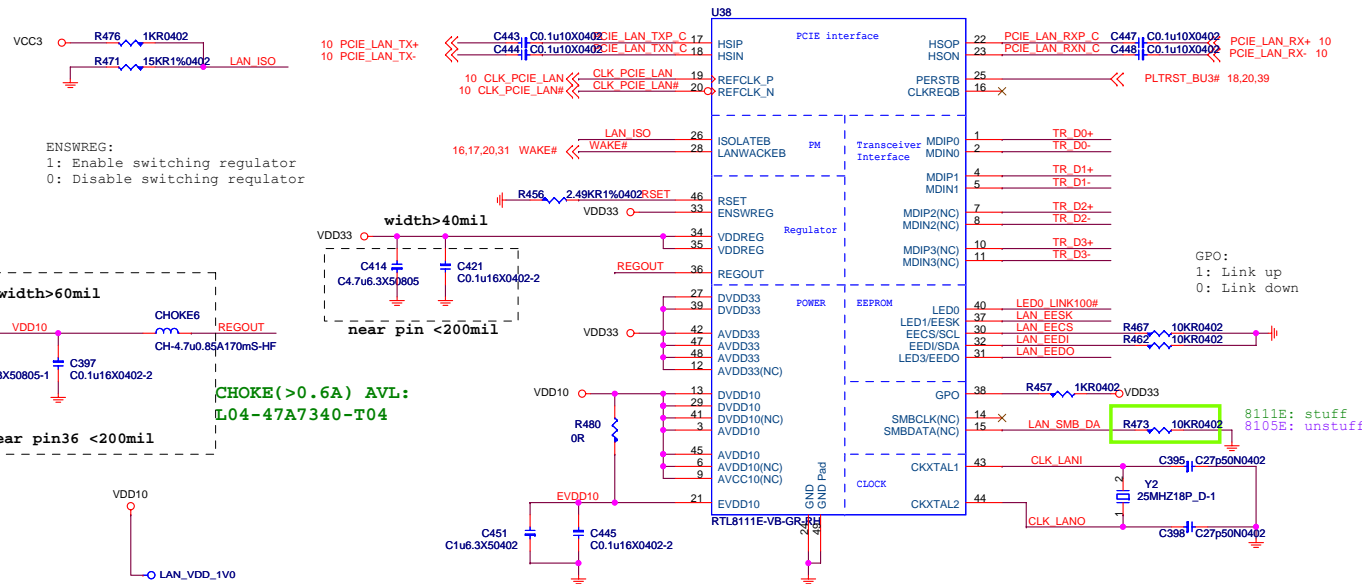


Rear 1394 port



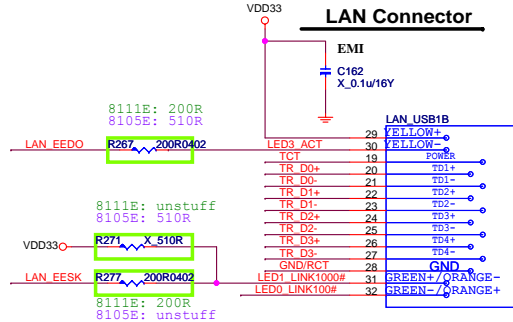
RTL8111E Giga LAN

RTL8105E 10/100M LAN



Pin49: 9 via from top layer to GND layer and make the via at the center of IC.

LAN Connector



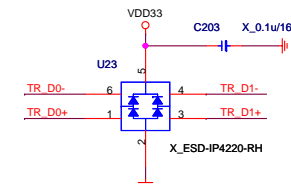
| Giga-Lan | 10/100-Lan |
|-----------------------------|-----------------------------|
| N58-22F0731 | N58-22F0771 |
| Link Yellow | Link Yellow |
| Active Blinking 1000 Orange | Active Blinking 1000 Orange |
| 100 Green | 100 Green |
| 10 None | 10 None |
| 19 | 19 |
| 20 | 20 |
| 21 | 21 |
| 22 | 22 |

8105E POWER Consumption

| | 3.3V | mW |
|-----------------|-------|---------|
| 10 M Idle/TxRx | 14/75 | 46/248 |
| 100 M Idle/TxRx | 43/66 | 142/218 |
| S0 ALDPS | 3.2 | 11 |

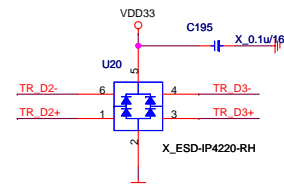
8111E POWER Consumption

| | 3.3V | mW |
|-----------------|---------|---------|
| 10 M Idle/TxRx | 12/66 | 40/218 |
| 100 M Idle/TxRx | 31/44 | 102/145 |
| Giga Idle/TxRx | 135/163 | 452/538 |
| ALDPS | 4 | 13 |

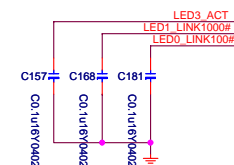


close to Connector

only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM



close to Connector

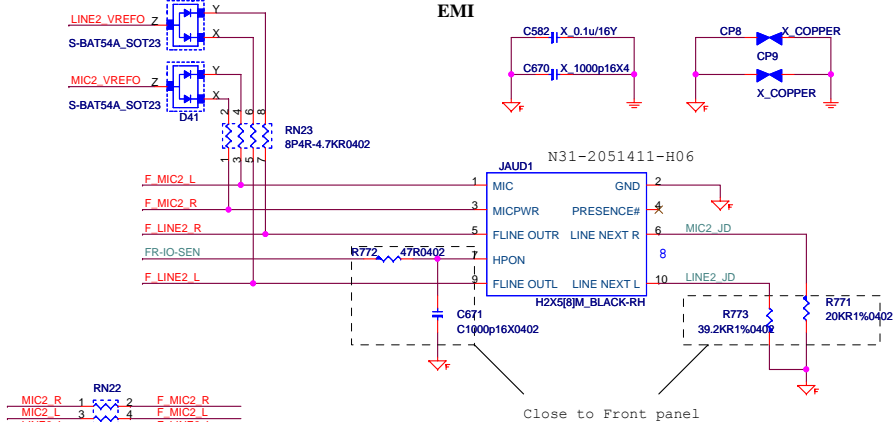
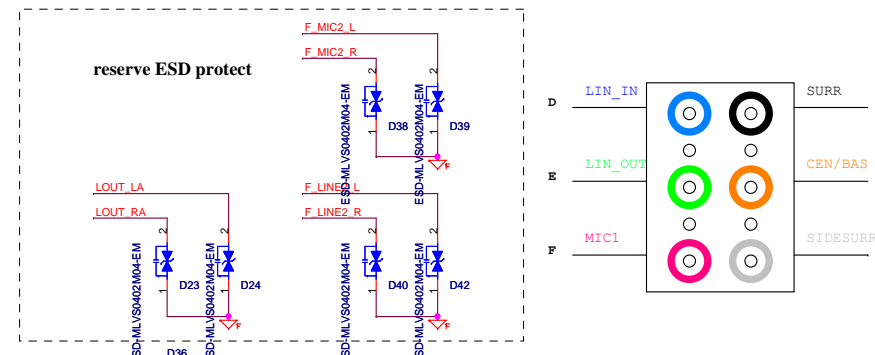
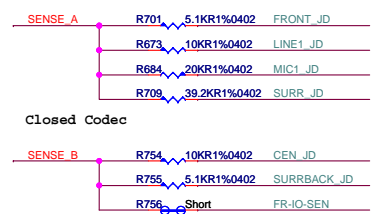
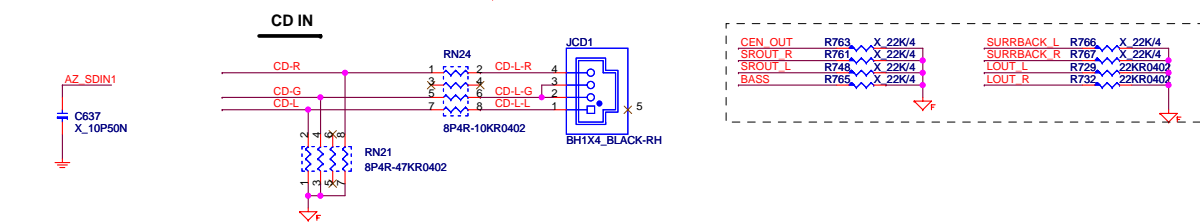


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| Size | Document Description | Rev |
|------------------------------|----------------------|-----|
| Custom | LAN - RTL8111E | 1.1 |
| Date: Monday, March 14, 2011 | Sheet 23 of 46 | |

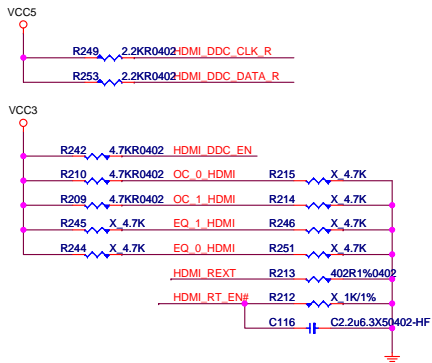
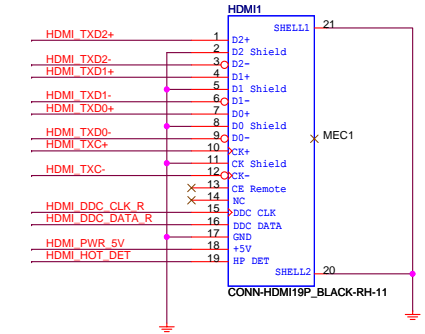
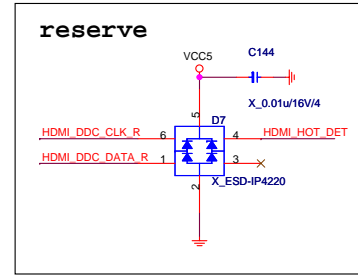
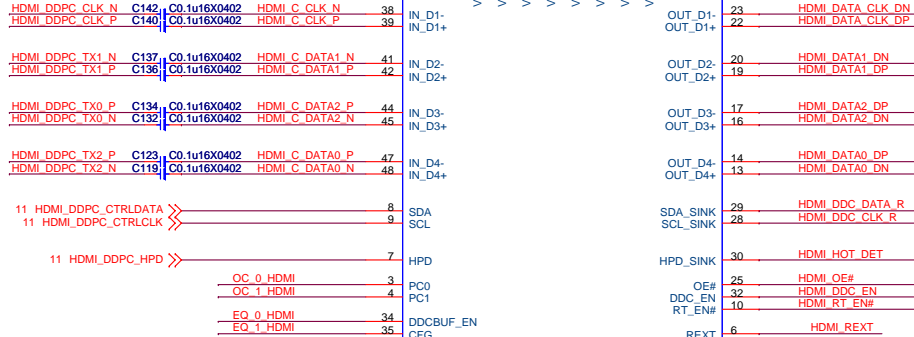
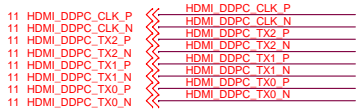
ALC892



MS-7678

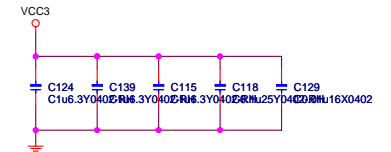
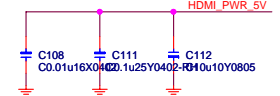
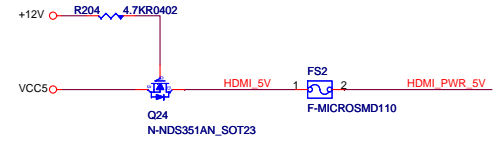
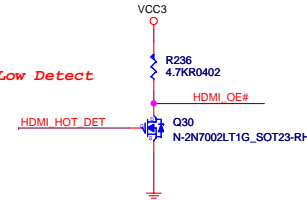
| | | |
|-------------------------------|--|----------------|
| Size Custom | Document Description ALC892_COLAY_ALC887VD | Rev 1.1 |
| Date: Tuesday, March 15, 2011 | | Sheet 24 of 46 |

HDMI level shifter



PERICOM 腹:B0B-411LS2C-P22.
PARADE 腹:B0B-081010C-P97.

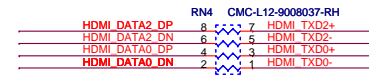
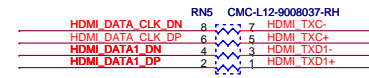
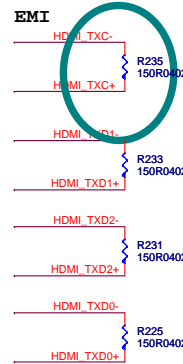
禁種High/Low Detect



| | "0" | "1" | note |
|-----------|--|---|---|
| DDC_EN | DDC level shifter disable | DDC level shifter enable | internal pull-up at ~500K ohm. |
| RT_EN# | Input 50 ohm termination resistor enable | the input termination ; resistors are set to high impedances | internal pull-down at ~500K ohm. |
| OE# | enable | the chip is power down and input termination resistors will be at high impedance. | internal pull-down at ~500K ohm. |
| HPD_SINK | disable | enable | internal pull-down at ~200K ohm; 5V tolerant. |
| DDCBUF_EN | For DDC level shifting configuration, please refer to Table. | | internal pull-down at ~500K ohm. |
| REXT | | | analog current generation. |

| [DDC_EN, DDCBUF_EN, OE#] | DDC Passive Switch | DDC Active Buffer |
|--------------------------|--------------------|-------------------|
| 1, 0, X | On | Off |
| 1, 1, 0 | Off | On |
| 1, 1, 1 | Off | Off |
| 0, X, X | Off | Off |

| PC1, PC0 | | note |
|----------|-------|----------------------------------|
| 00 | 8 dB | internal pull-down at ~500K ohm. |
| 01 | 4 dB | |
| 10 | 12 dB | |
| 11 | 0 dB | |



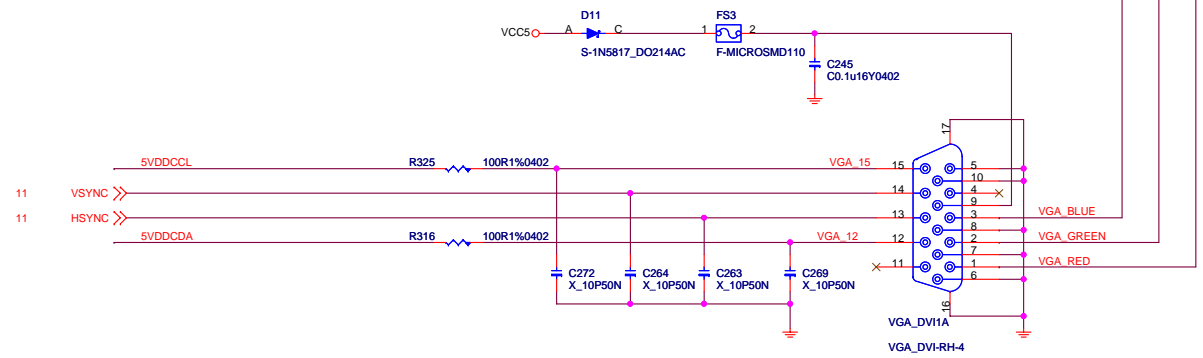
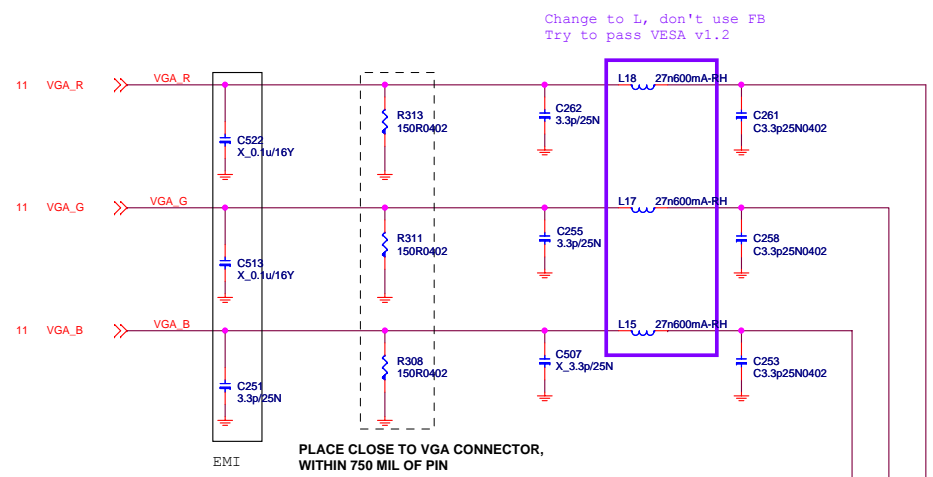
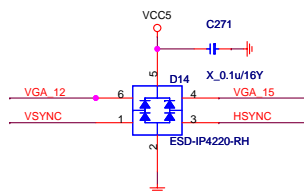
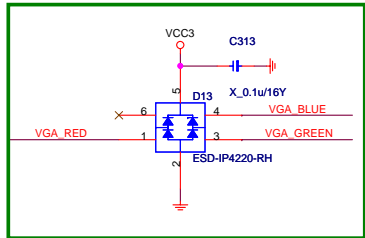
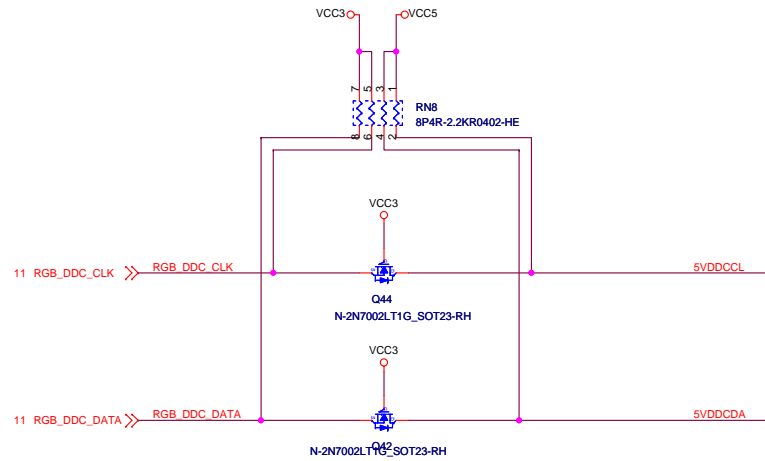
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| | | |
|------------------------------|---------------------------|---------|
| Size Custom | Document Description HDMI | Rev 1.1 |
| Date: Monday, March 14, 2011 | Sheet 26 of 46 | |

D-Sub

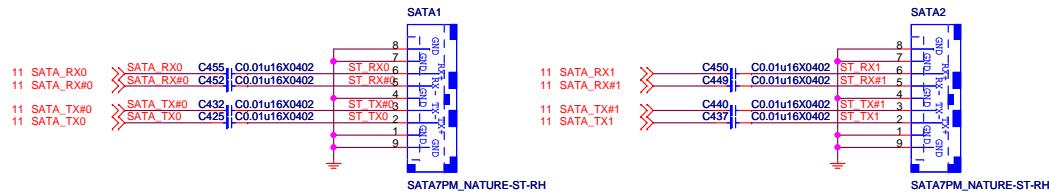
Levelshift





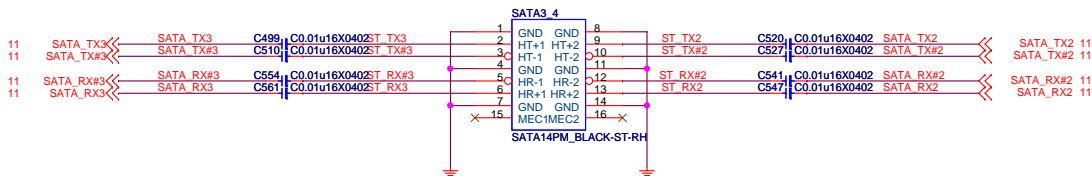
| MICRO-STAR INT'L CO.,LTD | | |
|------------------------------|----------------------|----------------|
| MS-7678 | | |
| Size | Document Description | Rev |
| Custom | VGA | 1.1 |
| Date: Monday, March 14, 2011 | | Sheet 27 of 46 |

SATA 6G PORT 0,1

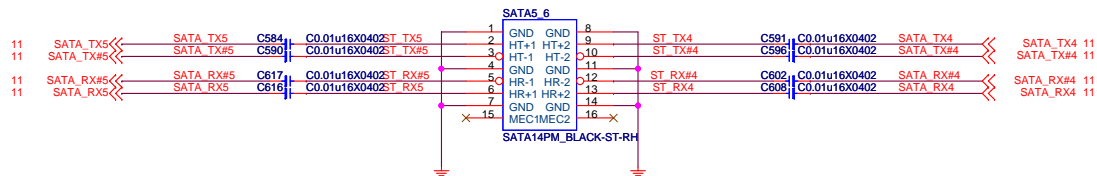


For B65,SATA2 should change to Gen2

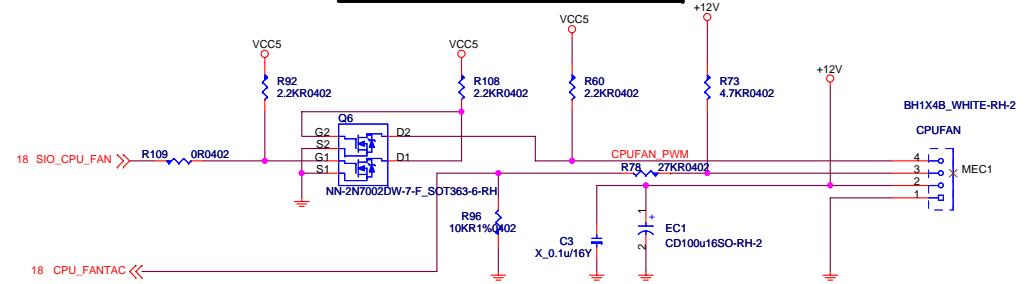
SATA 3G PORT 2,3



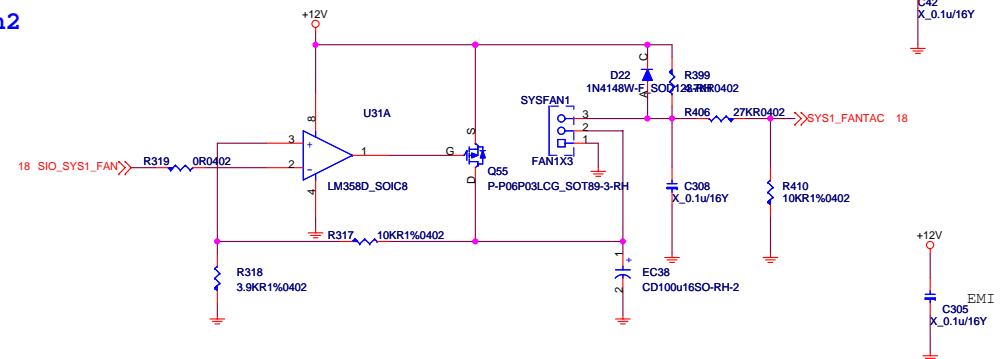
SATA 3G PORT 4,5



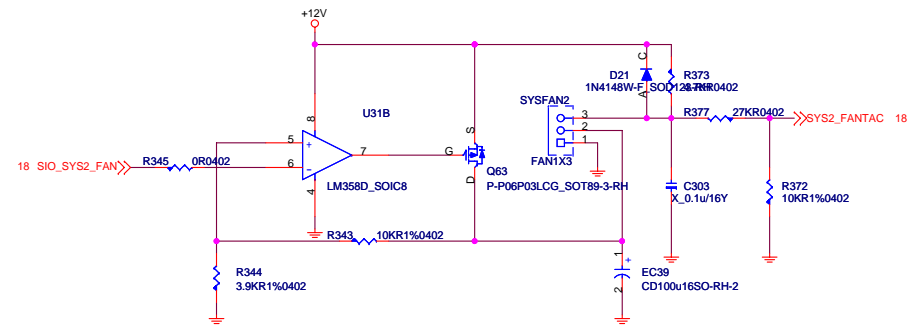
CPU FAN-COUNTROL CIRCUIT



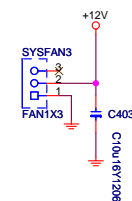
SYSTEM FAN1-COUNTROL CIRCUIT



SYSTEM FAN2-COUNTROL CIRCUIT

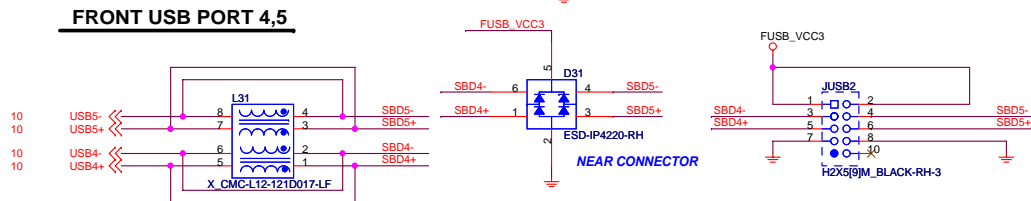
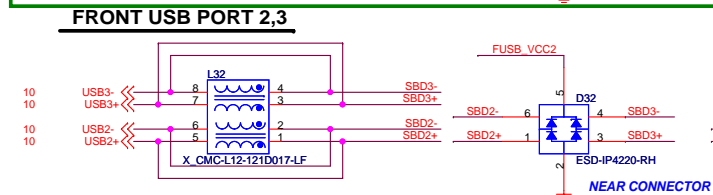
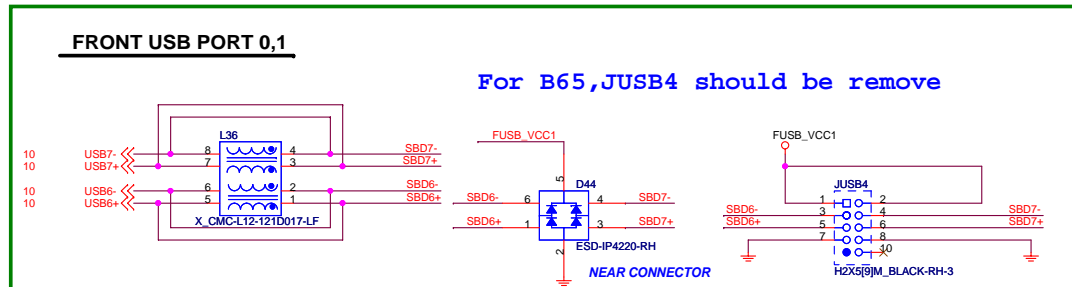
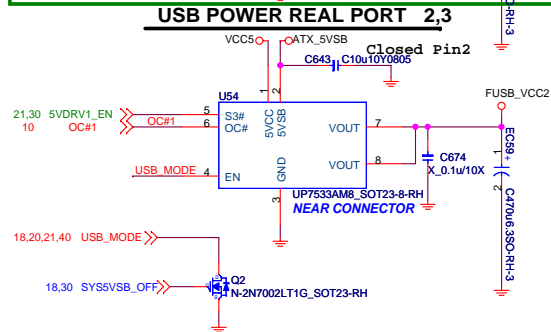
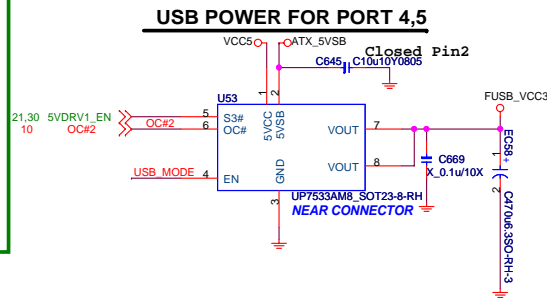
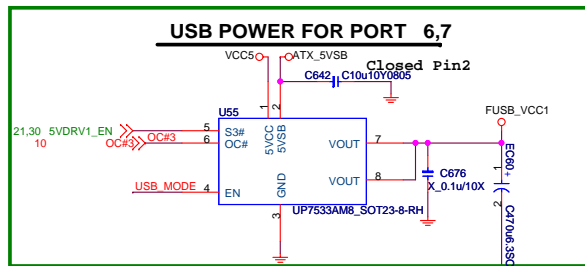


SYSTEM FAN3-12V

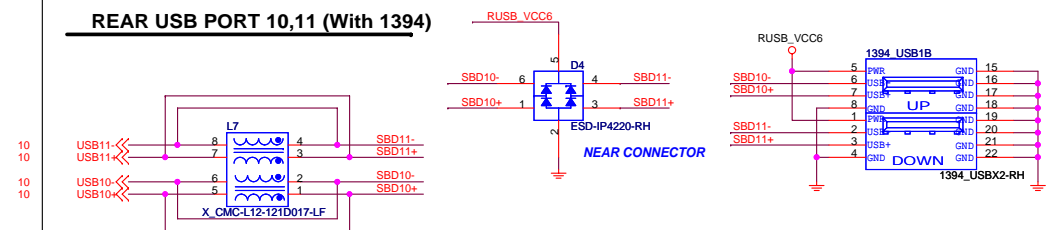
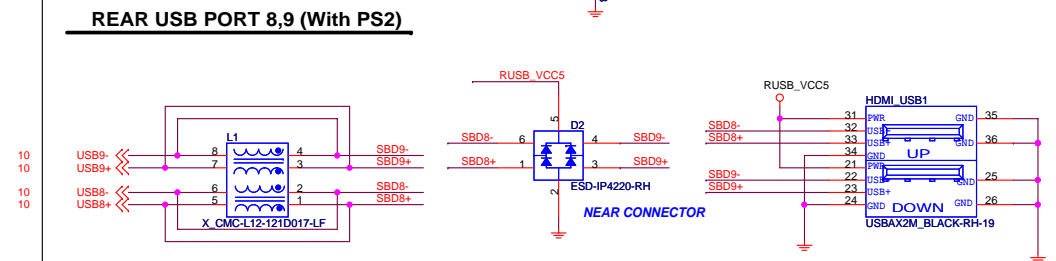
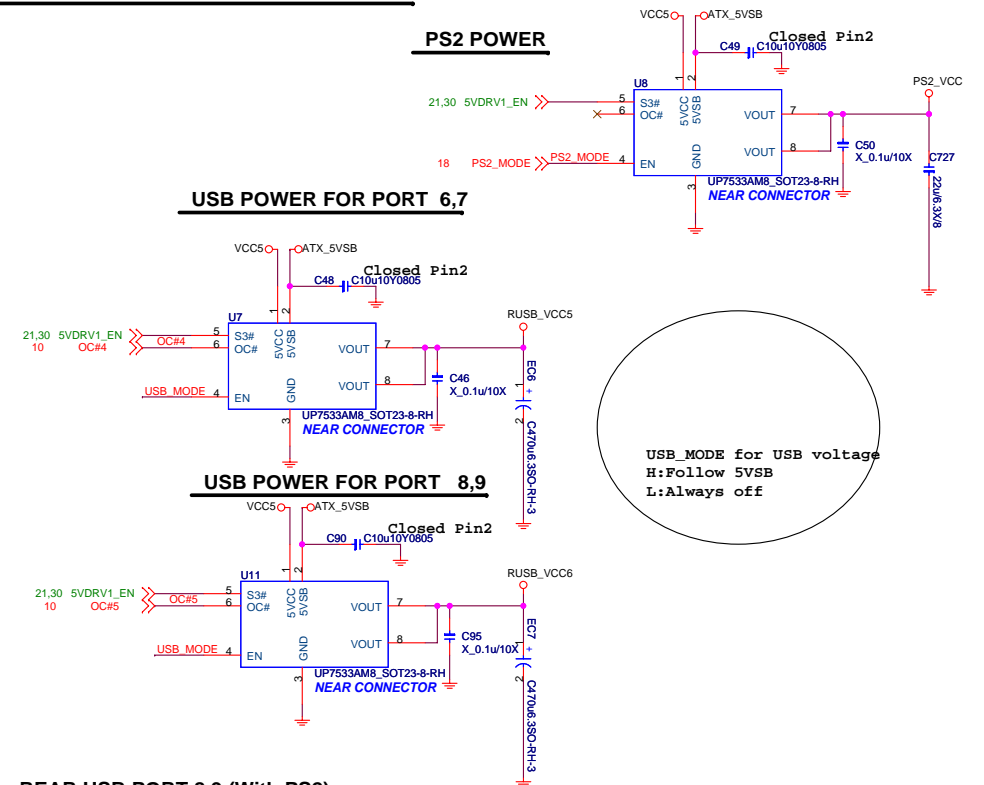


| MICRO-STAR INT'L CO.,LTD | | | |
|--------------------------|------------------------|-------|----------|
| MS-7678 | | | |
| Size | Document Description | Rev | |
| Custom | SATA / FAN Control | 1.1 | |
| Date: | Monday, March 14, 2011 | Sheet | 28 of 46 |

Front USB Connector



| |
|--------------------|
| Rear USB Connector |
|--------------------|

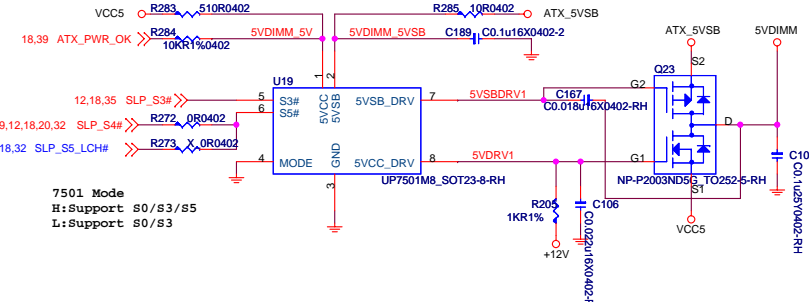


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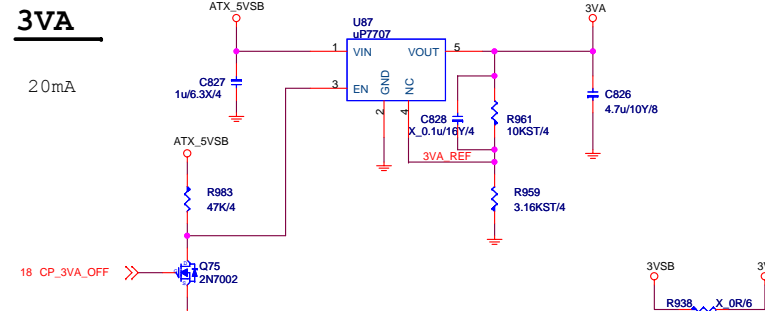
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|------------------------------|--|----------------|
| Size Custom | Document Description USB Connector | Rev 1.1 |
| Date: Monday, March 14, 2011 | | Sheet 29 of 46 |

5VDIMM FOR DDR

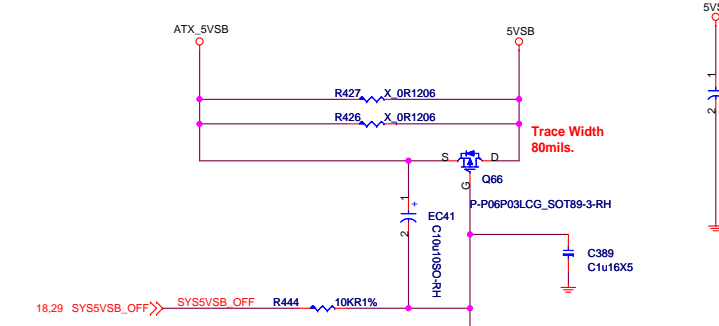


3VA

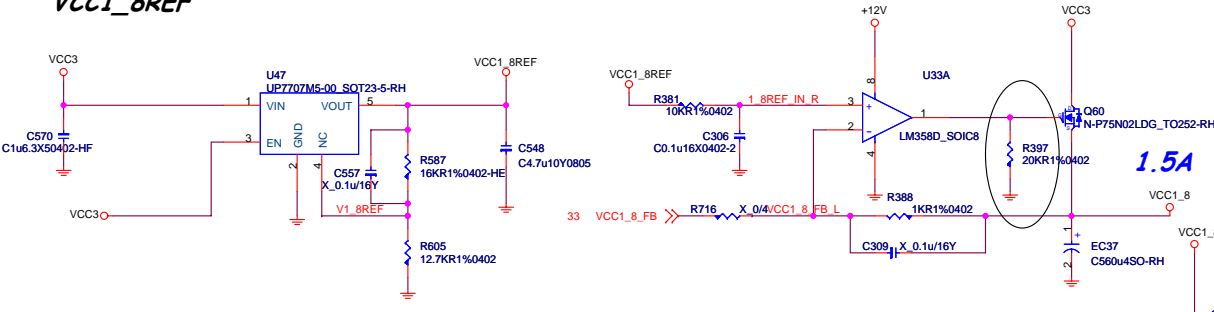
20mA



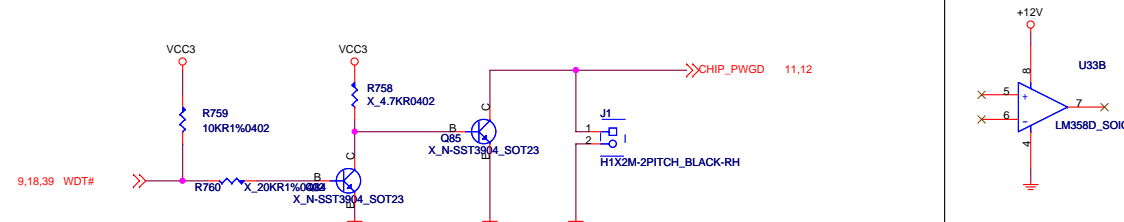
5VSB Power Switch



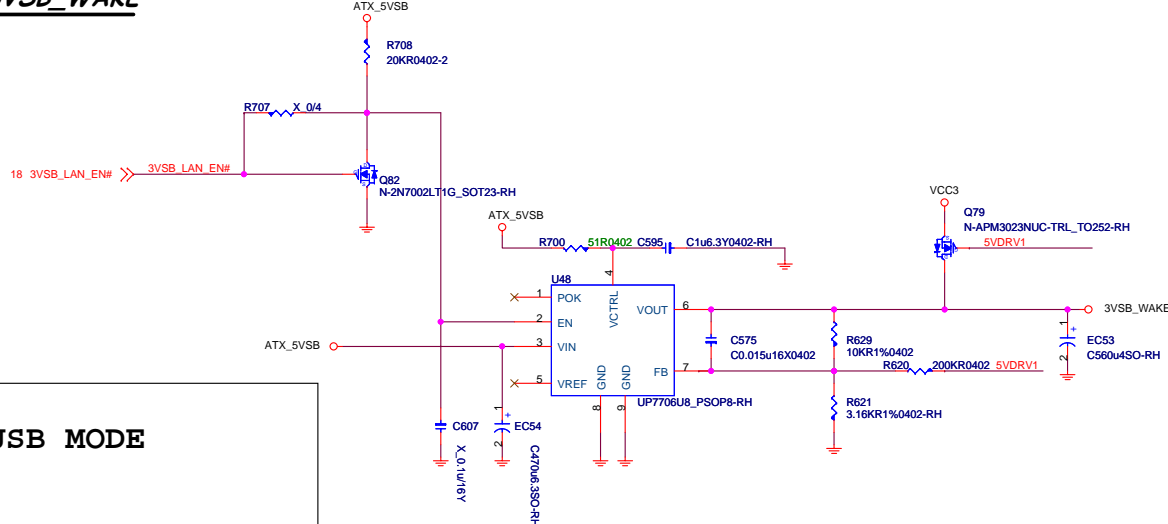
VCC1_8REF



WATCH DOG

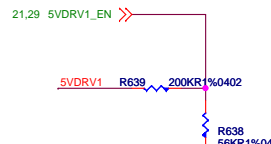


3VSB_WAKE



+3VSB WAKE supply to PCI Slot and LAN power.Turn off when Deep S3/S5 w/o WOL.

USB MODE

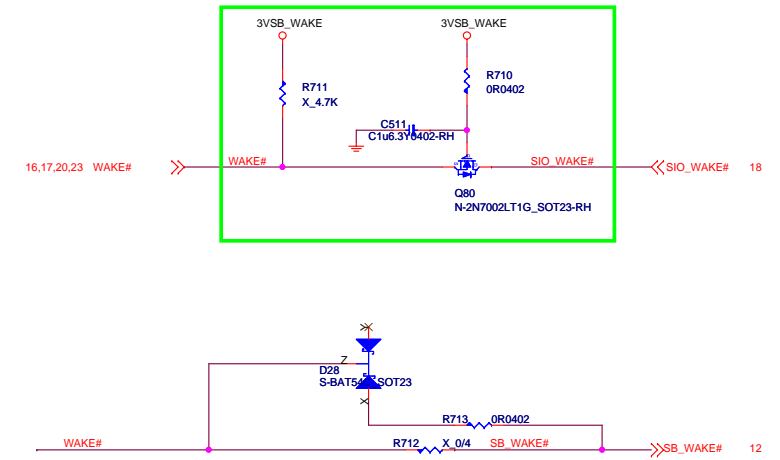


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| | | |
|-------------------------------|--|----------------|
| Size Custom | Document Description ACPI controller UPI | Rev 1.1 |
| Date: Wednesday, May 18, 2011 | | Sheet 30 of 46 |

LAN/PCIE/PCI Wake Up CTRL Circuit

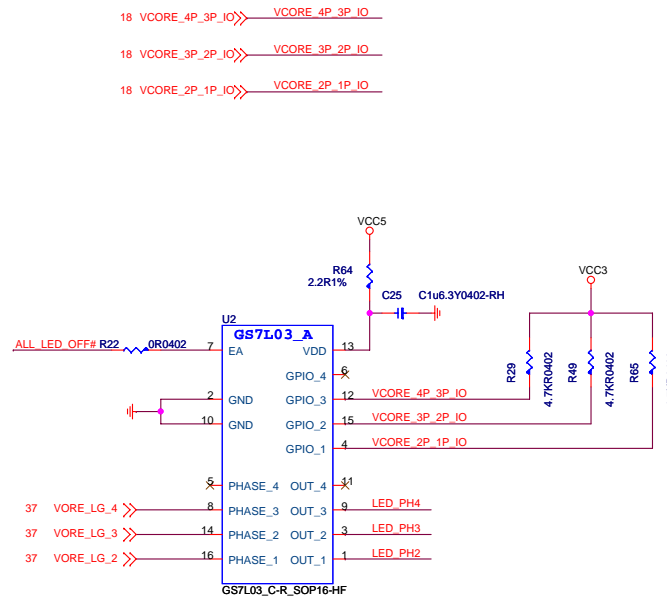


Power On

Hardware default = high

- 1.Set GPIO2_Data =1
- 2.Set GPIO2 port as output by open-drain mode
- 3.Porting GPIO2_Data =0 before system into deep_s3
- 4.Waiting CPU_PWRGD from low to high and setting GPIO2_Data =1 when resume from deep_s3

GPIO2 always keep high except for deep_s3



```
Power On
Hardware default = high
1.Set GPIO2_Data =1
2.Set GPIO2 port as output by open-drain mode
3.Porting GPIO2_Data =0 before system into deep_s3
4.Waiting CPU_PWRGD from low to high and setting
  GPIO2_Data =1 when resume from deep_s3

GPIO2 always keep high except for deep_s3
```

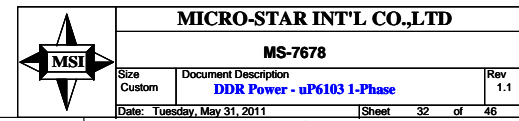
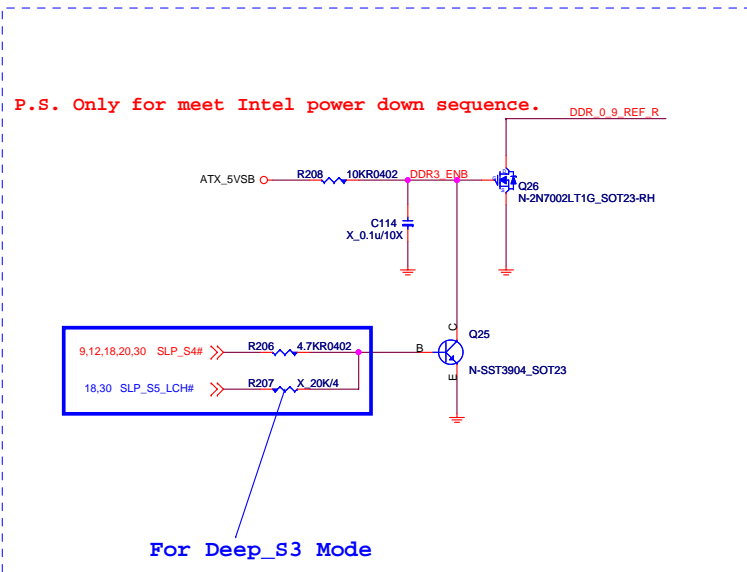


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| | | |
|-------------------------------|---|----------------|
| Size Custom | Document Description Power Saving circuit&APS | Rev 1.1 |
| Date: Wednesday, May 18, 2011 | | Sheet 31 of 46 |

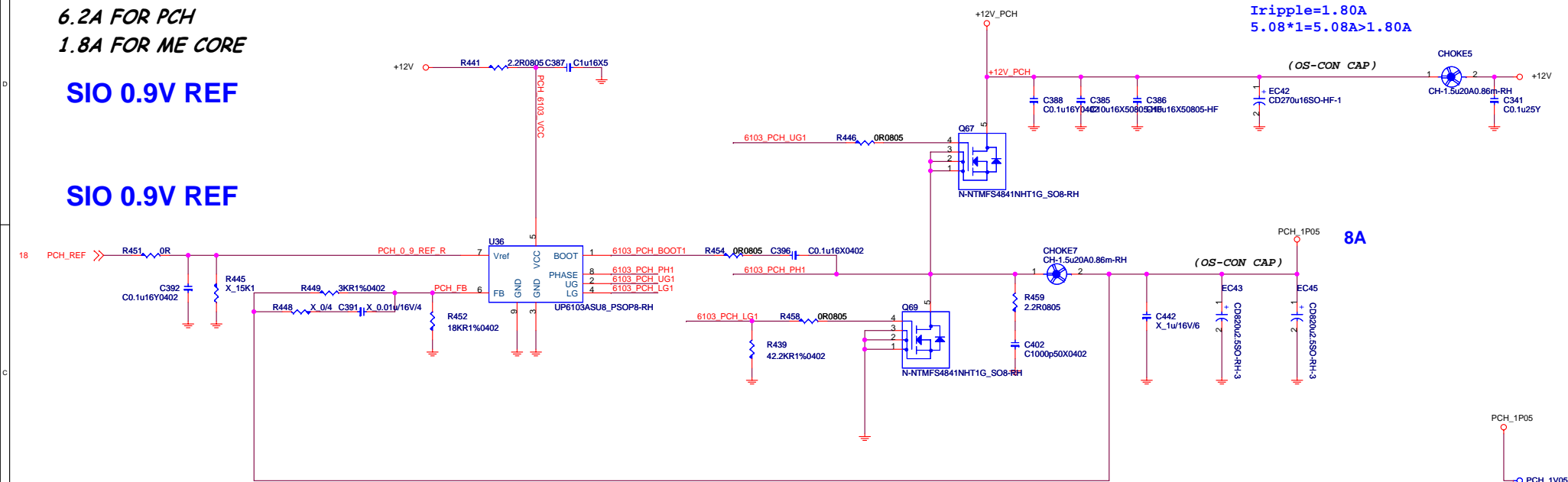
4.5A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

SIO 0.9V REF

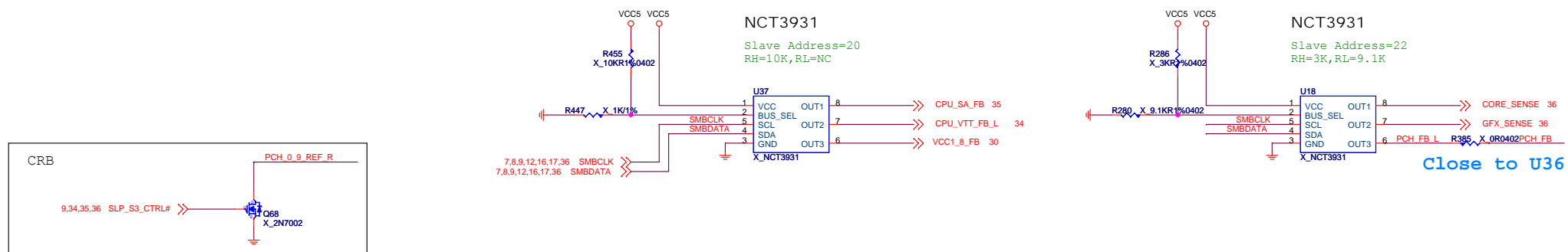


1.8A FOR ME CORE

SIO 0.9V REF



UPI VOLTAGE CONSOLE



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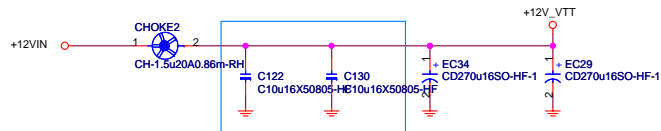
| | | |
|------------------------------|---|----------------|
| Size Custom | Document Description PCH Power - uP6103 1-Phase | Rev 1.1 |
| Date: Monday, March 14, 2011 | | Sheet 33 of 46 |

CPU_VTT:1.05/1.00

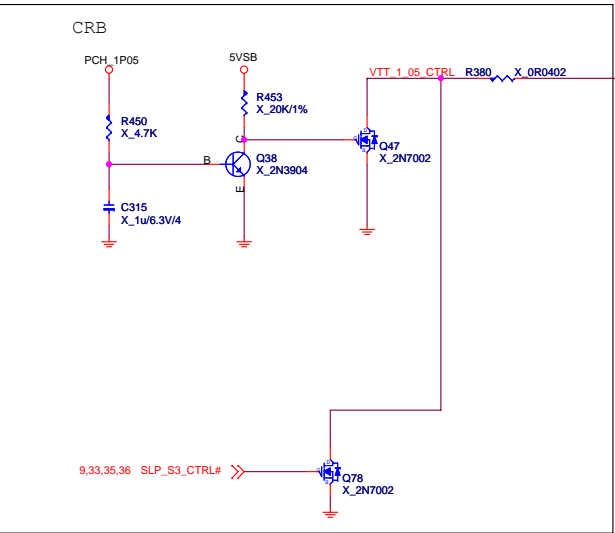
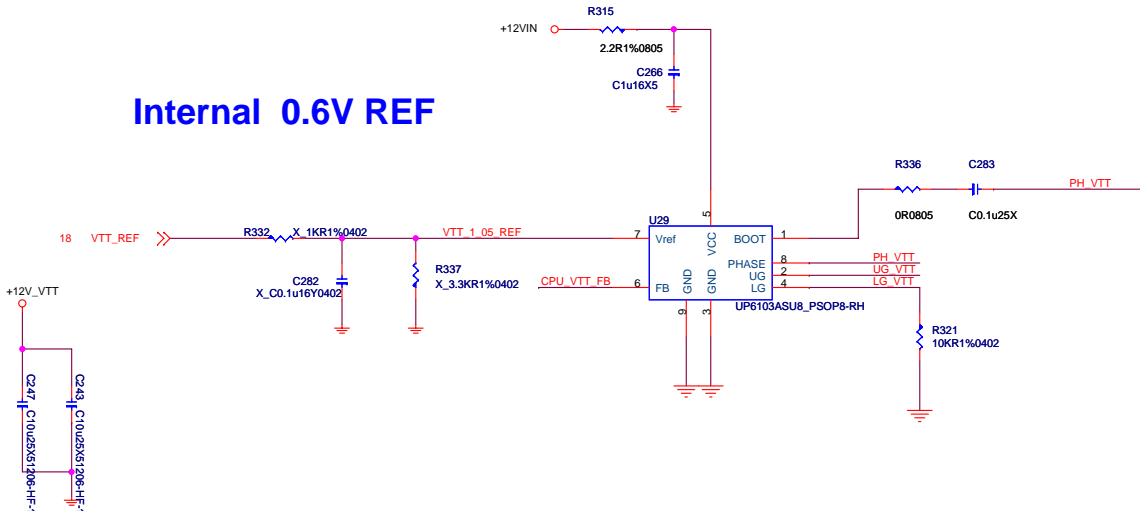
CPU VTT 8.5A

8.5A FOR CPU

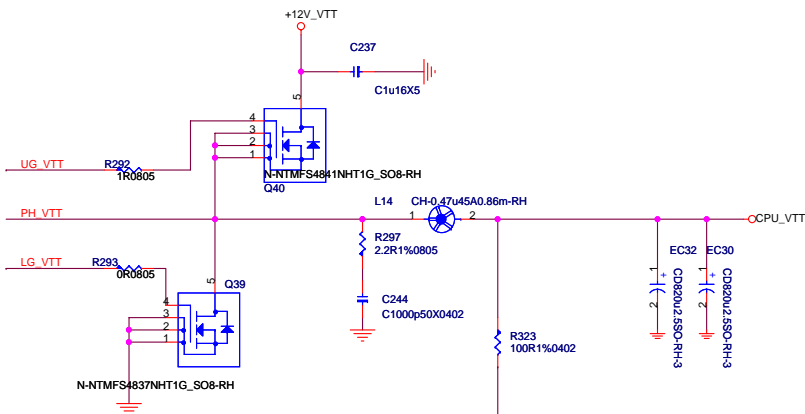
$I_{ripple} = 1.92(v_{tt}) + 1.88(sa)$
 $5.08 * 2 = 10.16A > 3.8A$



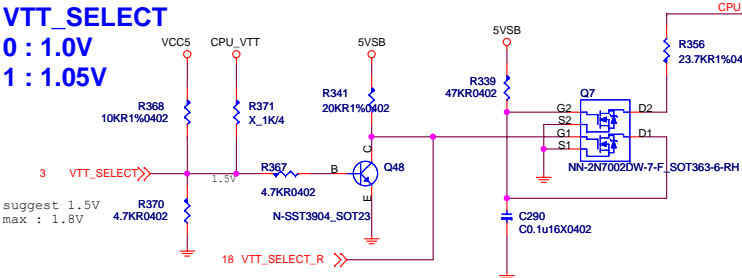
Internal 0.6V REF



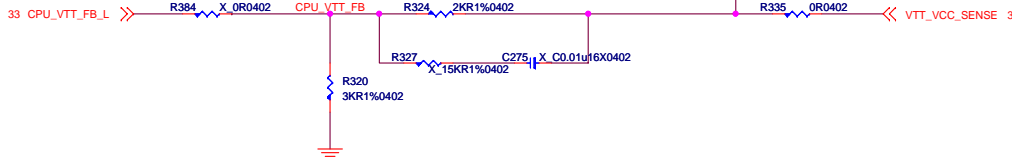
CPU_VTT
CPU_VTT_1V0



VTT_SELECT
0 : 1.0V
1 : 1.05V

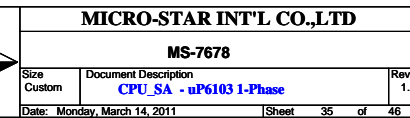
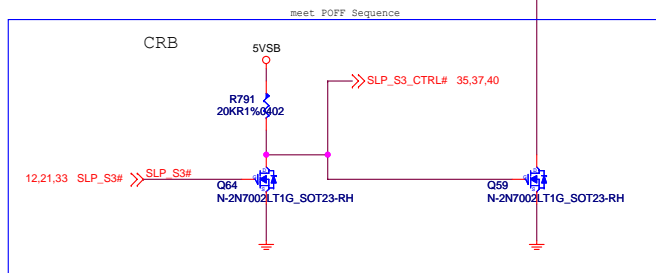


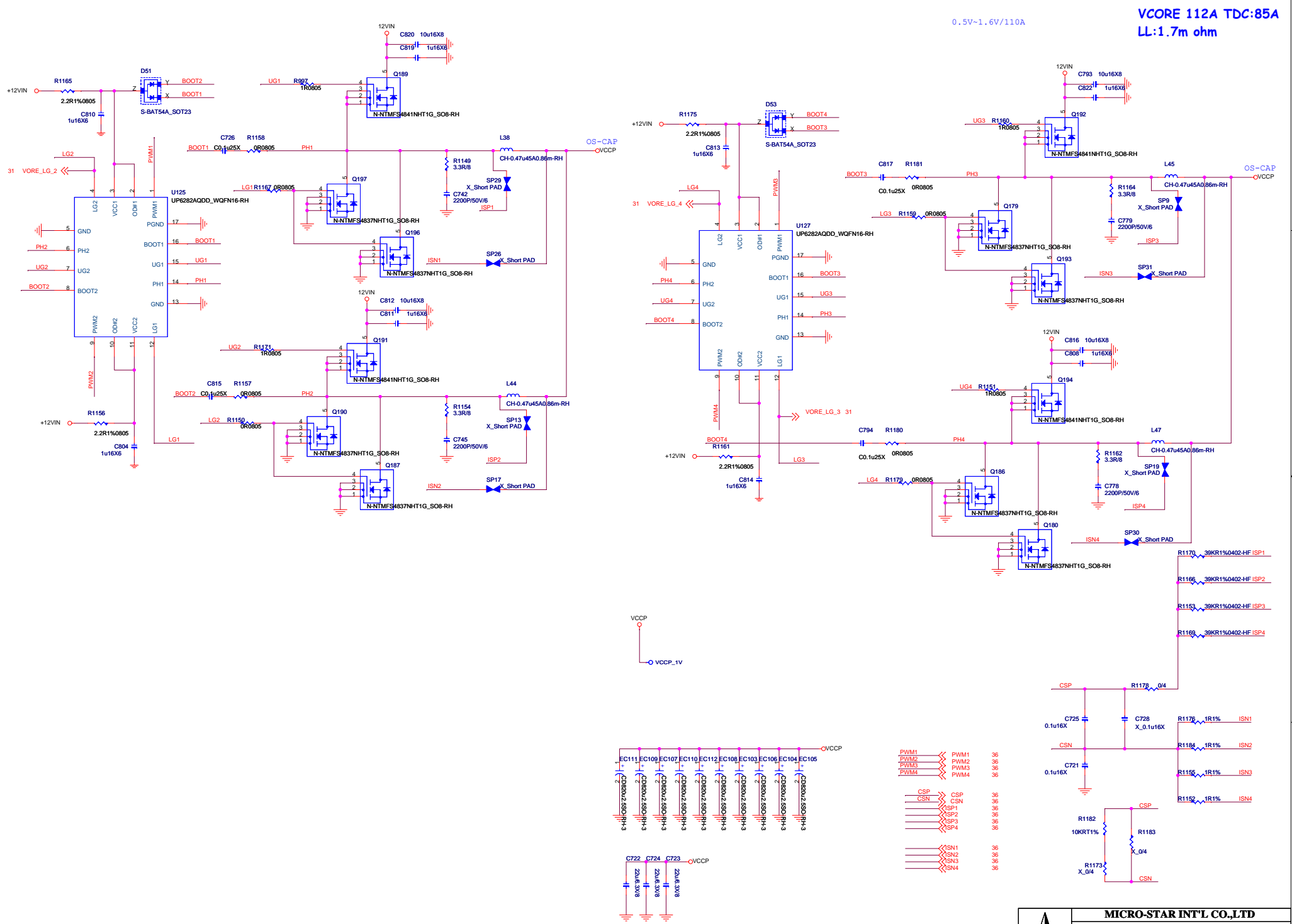
If use S10 ref, R356 should be 20K (R11-0203T12-W08)

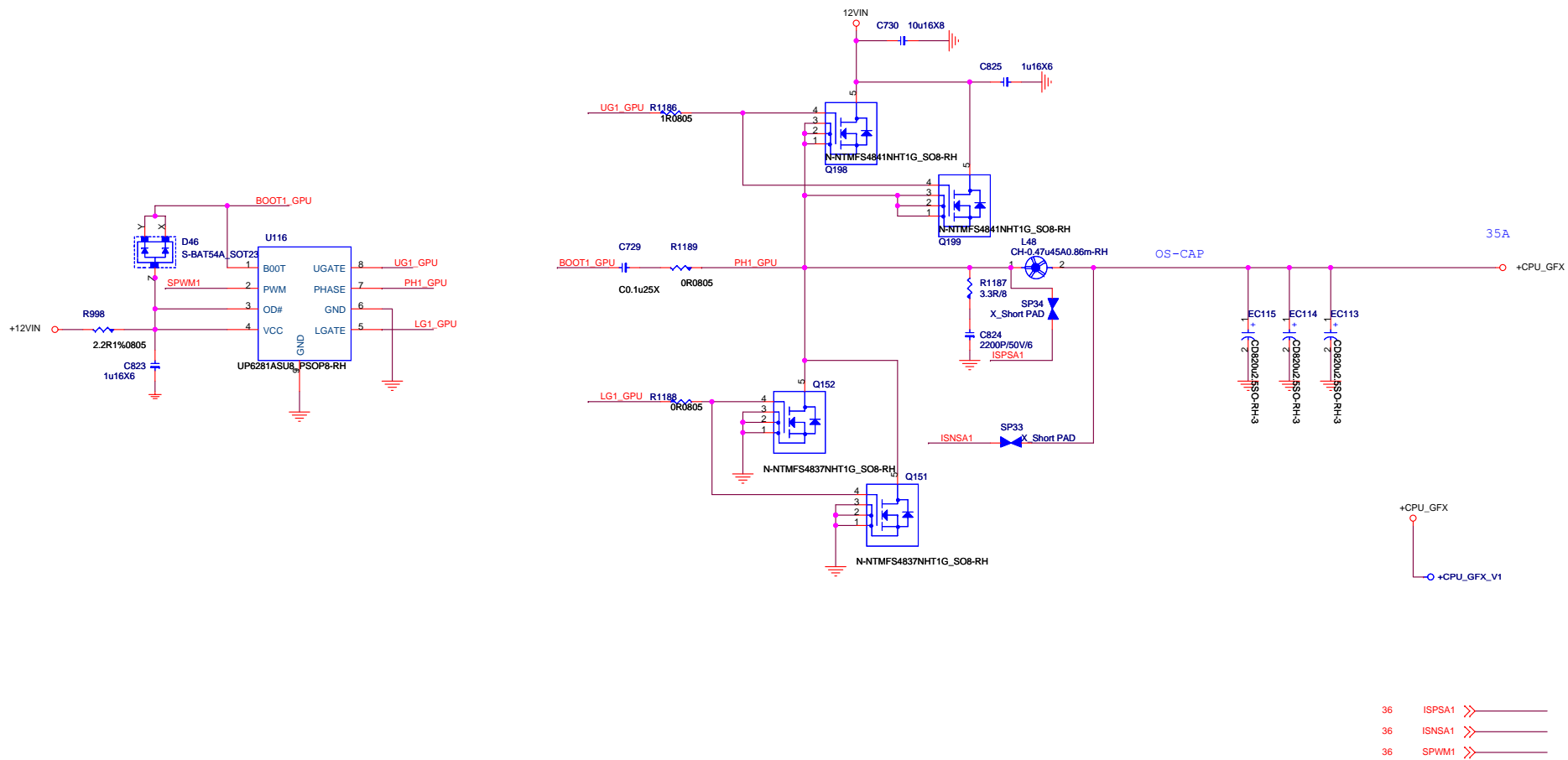


| | | | |
|--------------------------|--------------------------|-------|----------|
| MICRO-STAR INT'L CO.,LTD | | | |
| MS-7678 | | | |
| Size | Document Description | Rev | |
| Custom | CPU_VTT - uP6103-1-Phase | 1.1 | |
| Date: | Monday, March 14, 2011 | Sheet | 34 of 46 |

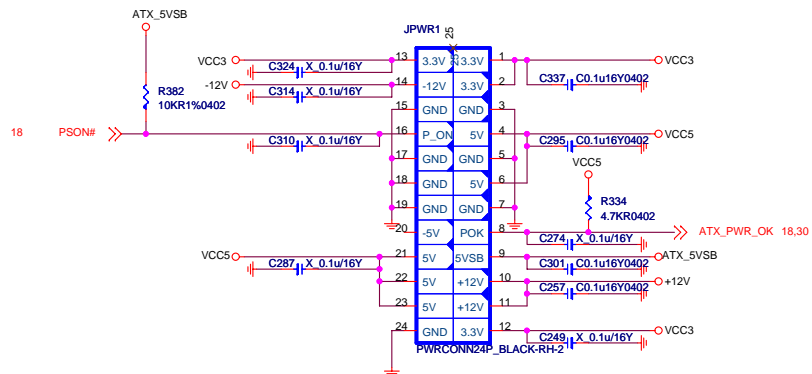
SA Core = 8.8A



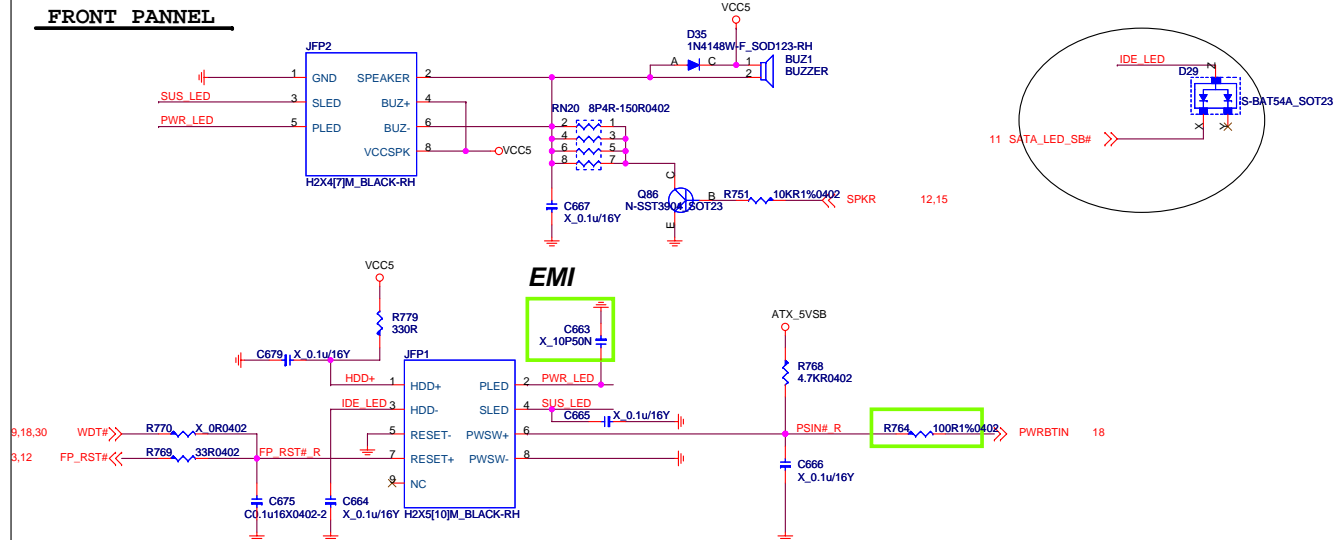




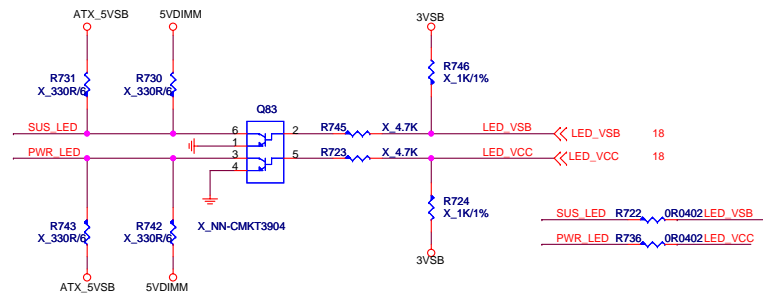
ATX POWER CONNECTOR



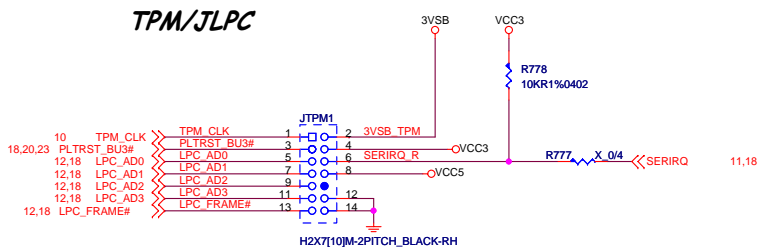
FRONT PANNEL



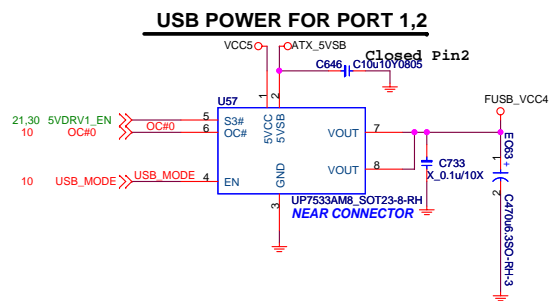
LED (for Fintek 71889)



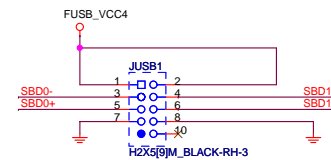
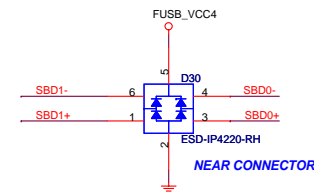
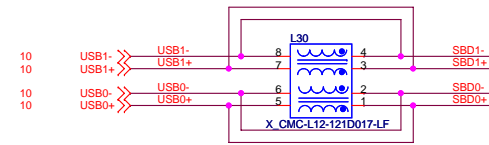
TPM/JLPC



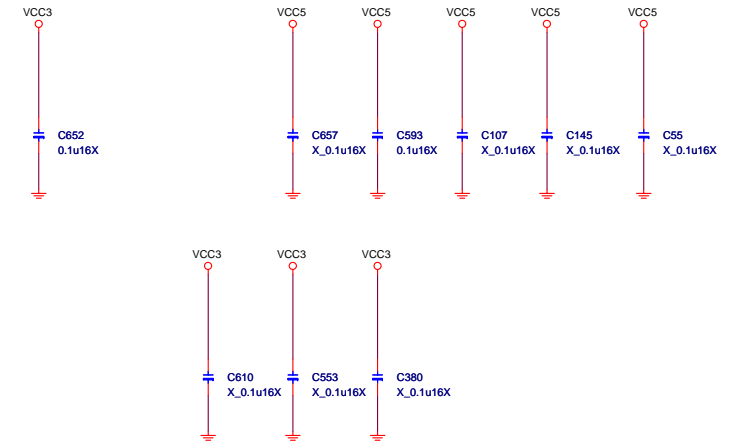
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|--------------------------|---------------------------------------|-------|----------|
| MICRO-STAR INT'L CO.,LTD | | | |
| MS-7678 | | | |
| Size | Document Description | Rev | |
| Custom | ATX PWR-Connector & Front Panel & EMI | 1.1 | |
| Date: | Friday, March 18, 2011 | Sheet | 39 of 46 |



FRONT USB PORT0.1



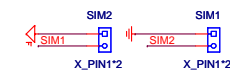
PCH XDP



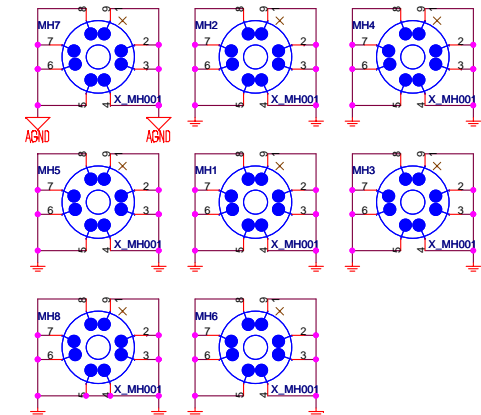
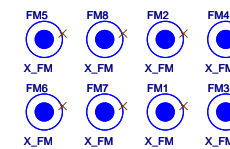
PCH XDP PWRGD/RESET

Mounting Holes

Simulation



Optical Fiducial Marks-120



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|-------------------------------|----------------------|-------|--|
| MS-7678 | | | |
| Size | Document Description | Rev | |
| Custom | XDP / Manual Parts | 1.1 | |
| Date: Wednesday, May 18, 2011 | Sheet 41 | of 46 | |